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Single-Electron Transistor (SET) Process and Device Simulation Using SYSNOPSYS TCAD Tools

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Abstract: Simulation of semiconductor device fabrication and operation is important to the design and manufacture of integrated circuits because it provides insights into complex phenomena that cannot obtained through experimentation or simple analytic models. Process and device simulation is commonly using for the design of new very large scale integration (VLSI) devices and processes. Simulation programs serves as exploratory tools in order to gain better understanding of process and device physics. In this research, single-electron transistor (SET) is simulated using Synopsys TCAD simulation tools to improve device performance and reliability or to increase the yield. The Taurus Medici is utilized for SET device simulation and the SET process simulation is utilizing Taurus TSUPREM-4. In addition, the structure of SET device, the capacitance, power, resistance and charging energy of SET device were obtained from these simulations. Ultimately, the SET device is operated at room temperature operation (300K).

Key words: Process simulation, device simulation, synopsys TCAD tools

INTRODUCTION

Computer simulations have emerged as a very elegant way to aid process and device engineers in their task of finding an optimum process. Process and device simulation is commonly use for the design of new very large scale integration (VLSI) devices and processes. Simulation programs serves as exploratory tools in order to gain better understanding of process and device physics[2]. On the other hand, simulations are also carried out after the design phase to optimize certain parameters of a technology, e.g., to improve device performance and reliability or to increase the yield[3]. The application of simulation tools in the development of new processes and novel device structures has become a worthwhile and an alternative to the experimental route[4].

For all these tasks the technology computer-aided design (TCAD)[2, 5-9] was coined. The present TCAD tools used in integrated circuits design can simulate the processes used today and predict the resulting device structure in one, two or three dimensions, eliminating the need for costly experiments[10]. In this study, we focused on the process and device simulation of single-electron transistor (SET) using Synopsys TCAD tools Taurus TSUPREM-4[11,12] and Taurus MEDICI[13,14] for SET simulation with nanowire length and nanowire width approximately 100nm and 10nm respectively.

Simulation tools: TCAD is computer-aided design and engineering used in semiconductor device design, fabrication process design, technology characterization for circuit design, manufacturing yield optimization and process centering, and computer-integrated manufacturing[15]. TCAD process and device simulation tools play a critical role in advanced technology development by giving insight into the relationships between processing choices and nanoscale device performance that cannot be obtained from physical metrology tools alone[16]. TCAD makes its greatest impact when a detailed understanding of the underlying physical mechanisms is tightly coupled within the technology development cycle so that physical insights feed directly into technology directions. The programs available in TCAD (especially Synopsys TCAD) are Taurus TSUPREM-4 and Taurus Medici.

Taurus TSUPREM-4 is an advanced one-dimensional (1D) and two-dimensional (2D) process simulator for developing semiconductor process technologies and optimizing their performance. With a comprehensive set of advanced process models, Taurus TSUPREM-4 simulates the process steps used for fabricating semiconductor devices, reducing the need for costly experiments using silicon[17]. In addition, Taurus TSUPREM-4 has extensive stress modeling capabilities, allowing optimization of stress to increase device performance[18]. Taurus TSUPREM-4 has the following capabilities[10,12,17,18]:

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* Design leading-edge MOS, bipolar, and power device manufacturing processes and devices.
* Predict 1D and 2D device structure characteristics by accurately simulating ion implantation, diffusion, oxidation, silicidation, epitaxy, etching, deposition and lithography processing.
* Evaluate and refine conventional and novel isolation technologies, such as local oxidation of silicon (LOCOS), deep trench and shallow trench isolation (STI).
* Investigate ion implantation processes, including the effects of wafer tilt and rotation on dose, shadowing, implant depth, and ion channeling.
* Study impurity diffusion, including oxidation enhanced diffusion (OED), transient enhanced diffusion (TED), interstitial clustering, dopant activation and dose loss.
* alyze stress history in all layers as a result of thermal oxidation, silicidation, thermal mismatch, etching, deposition, and stress relaxation at high temperatures.
* Determine basic electrical device characteristics, such as sheet resistance, threshold voltage and C-V curve (including quantum-mechanical connection).
* Create process structures for 2D and 3D device analysis using Taurus Medici and Davinci.

Taurus Medici is a powerful 2D device simulator that can be used to simulate the behavior of MOS and bipolar transistors and other semiconductor devices. With the most advanced physical models commercially available, Taurus-Medici allows device designs to be optimized for best performance without fabrication and eliminating the need for costly experiments[19,20]. In addition, Taurus Medici can be used to predict electrical characteristics for arbitrary bias conditions[14]. Taurus Medici has the following capabilities[13,10,19,20]:

* Analyze electrical, thermal and optical characteristics of devices through simulation without having to manufacture the actual device.
* Determine static and transient terminal currents and voltages of the device under all operating conditions of interest.
* Understand internal device operation through potential, electric field, carrier, current density, recombination and generation rate distributions.
* Optimize device designs without fabrication and find ideal structural parameters.
* Investigate breakdown and failure mechanisms, such as leakage paths and hot carrier (electron) effects.
* Generate data for compact model generation to allow analysis of circuit designs before processing.
* Use the Physical Model and Equation Interface (PMEI) to perform simulations that incorporate user-defined physical models and equations.

SIMULATION METHODOLOGY

Before doing the process and device simulation, the first step is to design the mask layout. This mask layout designed using Taurus Layout from Synopsys TCAD. Upon the completion of the mask layout design, the next step is process and device simulation.

Click on the computer to open the new terminal and then type the following quoted command: twb as shown in Fig. 1. A Taurus Workbench: Workspace window is opened (Fig. 2). Workspace is the top-level window display projects and network machine. Each project consists of a library and list of experiments. The Taurus Workbench (TWB): Workspace window is used as a main window for process and device simulation.

Then, create a new experiment which is in this experiment consists of process recipe and wafer flow as shown in Fig. 3.

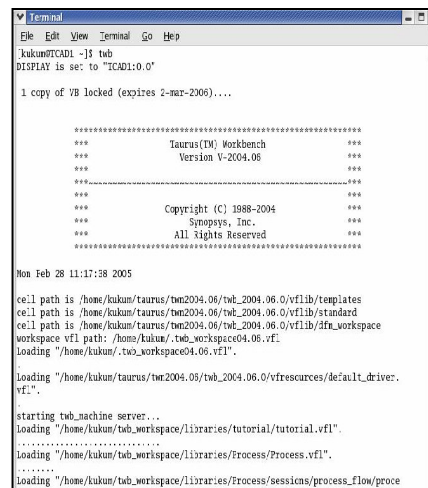

Fig. 1: Terminal window for taurus workbench

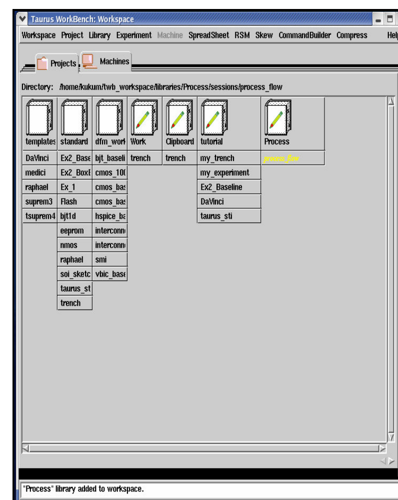

Fig. 2: Taurus Workbench (TWB): Workspace window

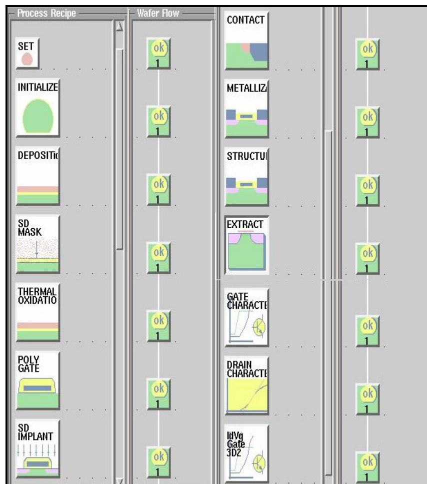

Fig. 3: TWB Experiment window for process and device simulation

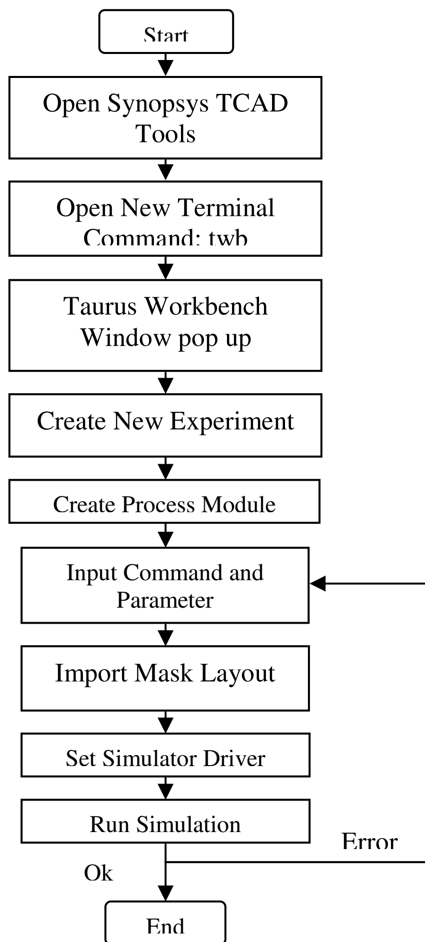

Fig. 4: The process and device simulation flow

By using an input command that suitable with the process module (e.g., initialize module used the initialize command), the wafer flow icon showed the 'ok' status of the module that mean the module successfully simulated. If used the wrong command, the wafer flow icon showed the error status with thumb down icon. The process simulation consists of ten modules which are initialize, deposition, source/drain mask, thermal oxidation, poly gate, source/drain implant, contact, metallization, structure, and extract. The device simulation have three modules are gate characteristics, drain characteristics, and gate characteristic three-dimensional simulation. The process and device simulation flow is shown in Fig. 4.

RESULT AND DISCUSSION

Mask layout is an input data for process simulation. The mask layout consist of four mask layers specially source layer, polysilicon gate layer, contact layer, and metal layer. These mask layout is designed using Taurus Layout from Synopsys TCAD. The complete mask layout for SET is shown in Fig. 5.

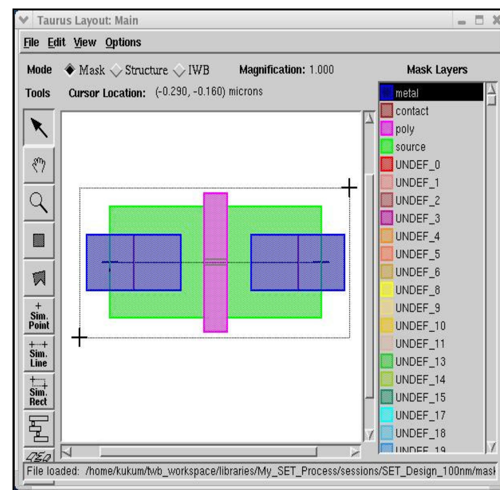

Fig. 5: Mask layout for SET simulation designed using Taurus Layout

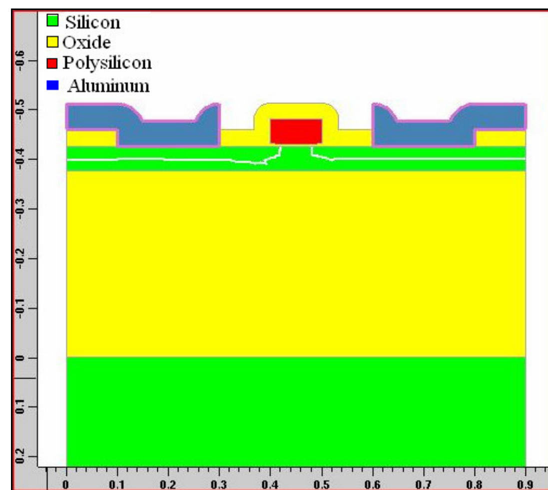

Fig. 6: Cross-section view of the device structure after completion of metallization process

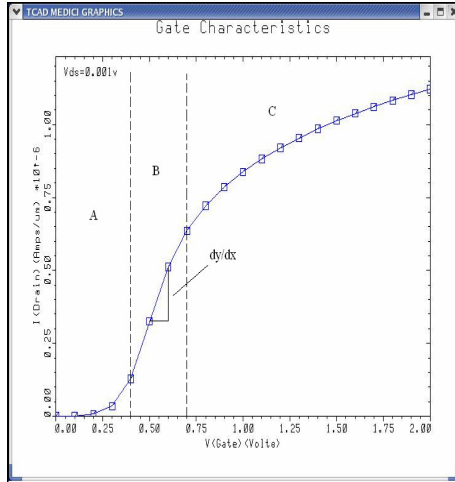

Fig. 7: Drain current, I_D as a function of the gate voltage, V_G

From Fig. 5, the layout is selected as a linear cut in a full layout for a two-dimensional simulation or a rectangular cut from the layout for a three-dimensional simulation[21]. The process simulation is to define the SET device structure and process parameter. After completed the process simulation, the device structure of SET is shown in Fig. 6.

The structure is next annealed at 450 °C for 30 seconds. The four electrodes such as source, drain, gate and substrate is defined. Once processing is completed, the finished structure (full transistor) is saved and will be used in Taurus Medici for device characteristics.

Then, the device characteristics of SET device are simulated employing Taurus TSUPREM-4 (process simulator) and Taurus Medici (device simulator). For gate characteristic, the drain current, I_D as a function of the gate voltage, V_G is shown in Fig. 5, for the SET made of silicon nanowire with a design length of 100 nm.

Here, the drain voltage was 1 mV, the source and substrate (back gate) voltages were fixed at 0 V and the device temperature was 300 K or 27 °C (room temperature operation).

As shown in Fig. 5, the graph is divided into three sections. In section A (from V_G at 0 V to V_G = 0.4 V), the drain current is increased immediately. At V_G = 0. 4 to V_G = 0.7 V (section B), the drain current increased linearly. While, in the section C when V_G is 0.7 V to 2.0 V, the drain current increased slowly.

Additionally, this graph is also given some information about this device. Firstly, the linear slope of this exponential graph is calculated. The linear slope is given by

$$\frac{dy}{dx} = \frac{y_2 - y_1}{x_2 - x_1} \qquad (1.1)$$

From the I_D-V_G graph (Fig. 5),

$$\frac{dy}{dx} = \frac{(5.2166\times10^{-7} - 2.8302\times10^{-7})A/\mu m}{(0.6-0.5)V} = 2.3864\times10^{-6} A/\mu mV$$

From this calculation, the linear slope is 2.3864 x 10^{-6} A/μmV. From the Ohm law,

$$V = IR, \qquad (1.2)$$

the resistance, R of SET device can be calculated. Based on the Ohm law, the resistance, R is

$$R_{SET} = \frac{V_G}{I_D} = \frac{1}{\frac{dy}{dx}} = \frac{1}{2.3864\times10^{-6}}\Omega = 0.4190\times10^{6}\,\Omega$$

From the calculation, the SET device resistance, R_{SET} is 0.4190 x 10^6 Ω. The power, P of SET device is given below,

$$P_{SET} = V_{SET} I_{SET} \qquad (1.3)$$

From Equation (1.2), $V = IR$, so the power is

$$P_{SET} = I^2 R_{SET} \qquad (1.4)$$

From Fig. 1.5, let say I = 3.0 x 10^{-7} A/μm hence

$$P_{SET} = [(3.0\times10^{-7} A/\mu m)^2]\times[0.4190\times10^{6}\,\Omega]$$

$$P_{SET} = 3.771\times10^{-8}\,Watt$$

$$P_{SET} = 0.3771\times10^{-9}\,Watt$$

The power, P for SET device is 0.3771 x 10^{-9} Watt for current is fixed. If voltage is fixed, let say V = 0.5 V, I = 2.8302 x 10^{-7} A/μm and R = 0.4190 x 10^6 Ω,

$$P_{SET} = [(2.8302\times10^{-7} A/\mu m)^2]\times[0.4190\times10^{6}\,\Omega]$$

$$P_{SET} = 3.3562\times10^{-8}\,Watt$$

$$P_{SET} = 0.33562\times10^{-9}\,Watt$$

So, power, P =0.33562 x 10^{-9} Watt. From the two calculations of power, the power, P of SET device is very low (10^{-9} Watt).

Based on the literature review, the threshold voltage, V_{TH} is

$$V_{th} = \frac{e}{C} \qquad (1.5)$$

From Equation (1.5), the capacitance, C of SET device can be calculated. From the I_D-V_G graph, V_{TH} = 0.3728 V at V_G = 0.5 V and e = 1.602 x 10^{-19} C. Hence, the capacitance, C is

$$C_{SET} = \frac{e}{V_{TH}} = \frac{1.602\times10^{-19}C}{0.3728V} = 0.4297\times10^{-18}F$$

The calculation showed capacitance, C = 0.4297 x 10^{-18} F or 0.4297 aF. As a result, the capacitance, C from the simulation result is 0.4297 aF at 300 K. Based on the previous experimental result done by Wasshuber, the capacitance, C is 3 aF at 300 K[22]. Another result done by Takahashi *et.al.*[23] is C = 2 aF at room temperature. Compare to two of the three results, the result from the simulation is smaller than the previous experiment done by others. The charging energy, E_C for SET is given below,

$$E_{C_{SET}} = \frac{e^2}{2C_{SET}} \quad (5.6)$$

From Equation (1.5), C_{SET} = 0.4297 x 10^{-18} F. Hence, the charging energy for this system is

$$E_{C_{SET}} = \frac{(1.602\times10^{-19})^2}{2(0.4297\times10^{-18})}$$

$$E_{C_{SET}} = \frac{2.9863\times10^{-20}}{1.602\times10^{-19}} eV$$

$$E_{C_{SET}} = 0.1864 eV = 186.4 meV$$

The calculation showed the charging energy, E_C for SET system is 186.4 meV at 300 K. Based on the previous reported about SET[24]; the charging energy is increased to 173 meV, which means that the transistor is able to operate at 300K. As a result, the value of charging energy from this calculation is nearly to the previous reported. Hence, the SET in this project is operated at 300 K.

In addition, the threshold voltage at 0.600 V gate bias is 0.3728 V and the channel length of the SET device is 61.27 nm. The simulation result shows that the sub threshold slopes for SET at 0.10 V gate bias is 112.3 mV/decade. The leakage current (I_{OOF}) at 0.0 V gate bias is 4.1715 × 10^{-12} A/μm. The drive current, I_{ON} is 0.034 μA/μm at $V_G = V_D$ = 1.5 V.

CONCLUSION

Technology CAD is the numeric simulation of semiconductor processes and devices. The use of computer simulations in the development of new processes has become a widely accepted technique to reduce the high cost and long turn-around times of real experiments. In this study, Synopsys TCAD tools are utilized for process and device simulation of SET. The simulation results showed the two-dimensional structure of SET from process simulation by using Taurus TSUPREM-4 and SET device characteristics from device simulation by using Taurus Medici. From the simulation, the threshold voltage for SET device is 0.3728 V which is operated at 300K (room temperature operation). From the calculation, the charging energy, E_C of SET system is 186.4 meV. The capacitance, C of SET device is 0.4297 aF and the power, P of SET device is 0.3771 x 10^{-9} Watt for fixed current and 0.33562 x 10^{-9} Watt if fixed the gate voltage. The power, P of this SET device is obtained from the I_D-V_G graph with fixed the resistance, R. The resistance, R is 0.4190 x 10^6 Ω. The value of capacitance that obtained in this simulation is smaller and the charging energy is higher than the previous reported.

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