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Design of Low Phase Noise SIPC based Complementary LC-QVCO for IEEE 802.11a Application

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Abstract: The paper presents the design of a source injection parallel coupled (SIPC) quadrature voltage controlled oscillator (QVCO), realized in a complementary architecture, which is usually preferred in low-power applications as it exploits ≈50% bias current reduction with double efficiency compared to the structure with single coupled, when operating in the current-limited regime. A stacked spiral inductor exhibiting a Q factor of 5.8, with pMOS based depletion mode varactor of 32% in tuning range, corresponding to 3.2-3.6GHz of tuning frequency, is implemented in 0.18µm CMOS technology. The phase noise of the SIPC QVCO architecture simulated at 1MHz of offset frequency is indicated to be -114.3dBc/Hz, while dissipating 11.0mW of core circuit power.

Key words: Phase noise, pMOS varactor, Quadrature voltage controlled oscillator (QVCO), Source injection parallel coupled VCO (SIPC-QVCO), Stacked spiral inductor

INTRODUCTION

Increasing demand for higher capacity in the growing LAN (WLAN) market has led to the introduction of a new generation of WLAN standards using more spectrally efficient modulation techniques. The 802.11a standards are based on orthogonal frequency division multiplexing (OFDM) modulation, where 52 uniformly spaced carriers are independently modulated with PSK or QAM, hence requires circuit architecture with low amplitude, high linearity and low phase mismatch, thus improved Error Vector Magnitude (EVM) performance. The standard supports data rates from 6 to 54Mbps in the 5GHz unlicensed national information infrastructure (UNII) band (5.15-5.35 GHz) [1].

In the transmitter the PA (Power Amplifier) output contains large spectral components in the vicinity of f_{LO}, leaking through the package and the substrate to the VCO and causing pulling. This effect is known as injection pulling [2]. To alleviate this effect proper frequency planning is utilized in the two-step up-conversion mixing action of the RF transmitter [3].

The accuracy in reported QVCO architecture designed utilizing a RC-CR polyphase filter is strongly dependent on the on-chip component matching, whereas the usage of frequency divider in realizing the QVCO topology increases the power consumption and results in quadrature inaccuracy due to any asymmetry in the duty cycle of the master-slave D-flip flop based frequency divider [4]. A cross coupled QVCO topology is exploited to enhance the phase accuracy. In this paper a SIPC based QVCO topology is adapted [5]. By alleviating the noise current flow through the switching transistor from the coupling transistor the up conversion of the $1/f$, flicker noise is relaxed.

A stacked spiral inductor with comparable Q-factor and self resonant frequency is designed [6] and integrated into the QVCO architecture to provide frequency tuning via the LC tank configuration. A metal6-metal4 stacked rectangular spiral inductor which provides self shielding effect is implemented and extracted utilizing ASITIC (Analysis and Simulation of Inductors and Transformer for IC's) tool.

A pMOS based capacitor with drain, source and bulk (D,S,B) connected together [7], realizes the frequency tuning of the LC tank. Both in accumulation

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and inversion region of operation the MOS capacitor exhibit a maximum of oxide capacitance, $C_{ox.}$

This paper is organized as follows. The frequency planning scheme description for IEEE 802.11a application is followed by the review on the design of the stacked spiral inductor, subsequently by the utilized pMOS based capacitor and the description of the integrated complementary based SIPC-QVCO architecture. Simulation results on the realized SIPC based QVCO in 0.18µm CMOS technology is reported prior to the presented conclusion.

FREQUENCY PLANNING

Figure 1 reports an LO generation scheme utilized in realizing two step up-conversion transmitter in compliance with IEEE 802.11a application. The voltage controlled oscillator (VCO) operates at two thirds of the LO frequency and a divide by 2 circuit produces quadrature outputs at one third of LO frequency. As the VCO operates at two thirds of the LO frequency, this scheme effectively suppresses the injection pulling effect and LO-RF interaction by subsequent stage of PA. The generated LO signal has a cleaner frequency content at the LO frequency, minimizing the adverse effect of the unwanted sideband [8].

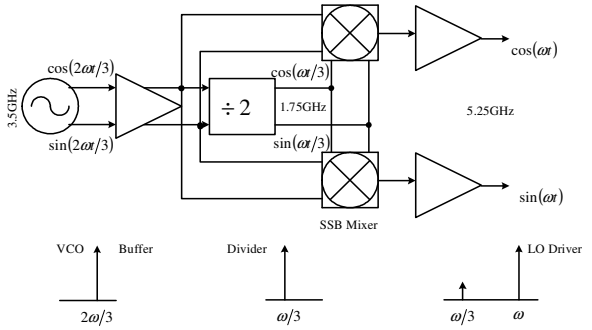

Fig. 1: Proposed frequency planning for IEEE 802.11a Transmitter architecture [6]

ARCHITECTURE AND CIRCUIT IMPLEMENTATION

Stacked Spiral Inductor: Figure 2 illustrates the vertical cross section of the realized stacked inductor, with the indication of substrate and oxide thickness. Figure 3(a) illustrates the layout view of the designed inductor with patterned grounded shield (PGS), which terminates the induced electric field and prevents it from reaching the substrate. Figure 3(b) describes the equivalent circuit model with PGS [6],

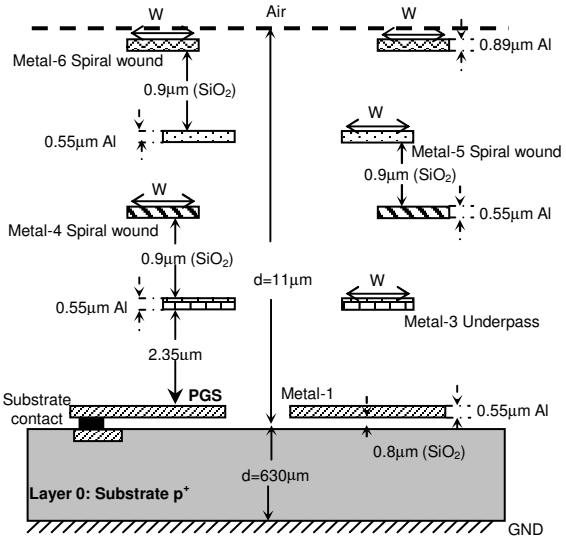

Fig 2: Spiral inductor cross section showing various layers metal 6 to metal 4 is used for creating the turns of the spiral with an underpass layer of metal 3. The PGS is designed in metal 1.

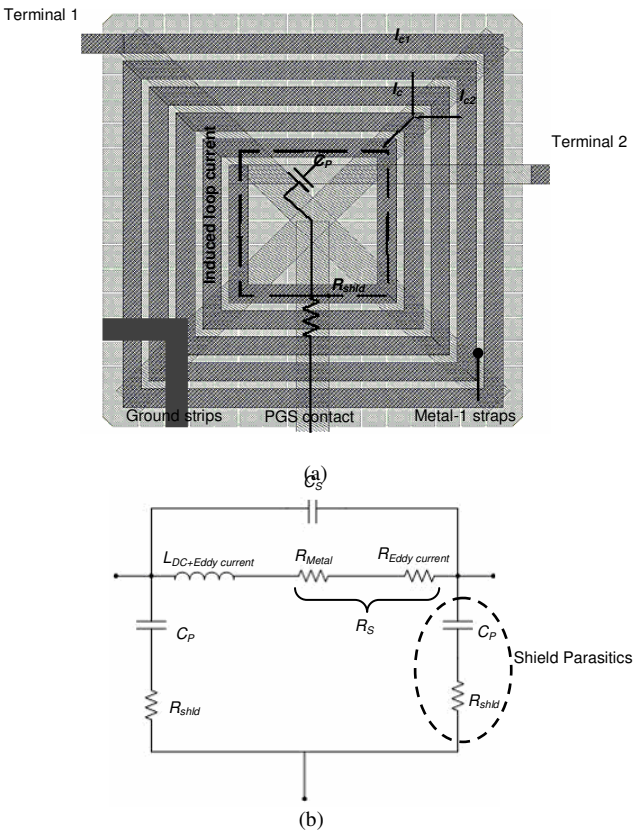

Fig. 3: Stacked spiral inductor (a) layout view with PGS, metal 1 straps and substrate parasitic distribution and (b) equivalent circuit model.

where $L_{DC+Eddy\ current}$, is the equivalent inductance due to the dc self inductance and mutual coupling inductance, R_{Metal} and $R_{Eddy\ current}$, denotes the dc metal line and reverse eddy current induction losses, respectively, C_S is the series capacitance due to the effect of interwinding and overlapping capacitance effect, whereas C_p and R_{shld} are the shield parasitics.

pMOS Varactor

The gate of the device is defined as anode v^+, while the source, drain and bulk are tied together, forming the cathode, v^-, of the device as described in Figure 4. The varactor gate sided tuning is used to alleviate leakage.

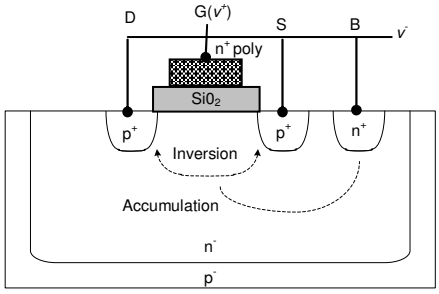

Fig. 4: pMOS cross section describing MOS capacitor in inversion, depletion and accumulation regions.

Inversion channel with mobile holes builds up for $V_{BG}>|V_T|$, where $|V_T|$ is the threshold voltage of the transistor, resulting in an equivalent capacitance, C_{ox} [7]:

$$C_{ox} = \frac{\varepsilon_{ox} A}{t_{ox}} \quad (1)$$

where A and t_{ox} are the transistor channel area and oxide thickness, respectively.

The depletion mode with very few mobile charge carriers, results in a decrease of the equivalent capacitance to $C_{ox}+C_d$, where C_d is the series depletion mode capacitance. The varactor Q is defined by [7]:

$$Q = \frac{1}{\omega C_V R_V} \quad (2)$$

where R_V is the series parasitic resistance including the channel resistance and gate resistance, which is reduced utilizing minimal length double sided tapped gate MOS varactor with multi finger realization. C_V describes the varactor capacitance, where $C_V=C_{ox}.W.L.nf$, in which W, L and nf corresponds to the width(μm), length(μm) and number of fingers of the varactor, respectively.

Complementary Based SIPC-QVCO

Figure 5 shows the schematic of the complementary based SIPC-QVCO topology. In contrary to the conventional QVCO architecture, the drain node A of the coupling transistor, M_{C1}-M_{C4} are connected directly to the ground (GND) terminal.

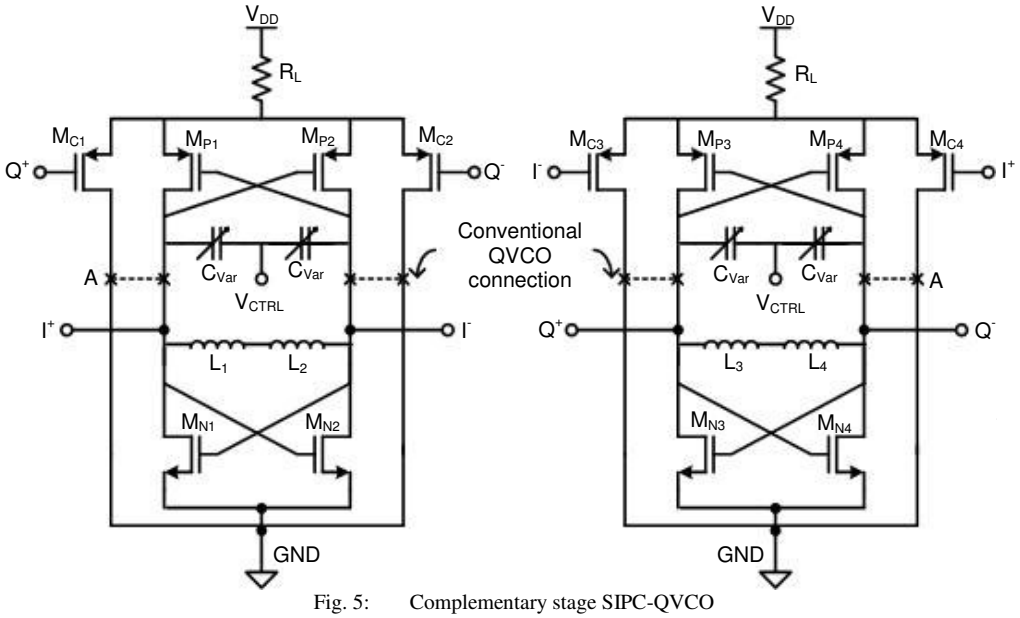

Fig. 5: Complementary stage SIPC-QVCO

Phase noise in the $1/f^3$ region is primarily dependant upon the up-conversion of flicker noise from the MOS switching transistors, M_{N1}-M_{N4}. Bias current noise has been observed to be a dominant contributor to phase noise in the $1/f^2$ region, solutions are filtering and removing the bias current generator where filtering requires large inductors and capacitors, while removing current source increases sensitivity to power supply noise and variation of the bias current over process and temperature, hence the utilization of common mode resistor to the biasing supply voltage is preferred. There is no particular reason in choosing an nMOS or a pMOS device with regard to $1/f^2$ phase noise in selecting the coupling transistor pair, largely because the device have been assumed to yield equivalent thermal noise for an equivalent g_m. The reduction in $1/f^3$ phase noise is fundamentally limited by switching transistors $1/f$ noise [9].

In a conventional QVCO architecture, the resulting $1/f$ noise current flows through the switching transistor M_{N1}-M_{N4}. When the coupling transistors turns off, the abrupt change in noise current leads to a voltage induction across M_{N1}-M_{N4}, which up-converts the $1/f$ noise to the frequency of oscillation, thus degrading the phase noise performance [5]. The SIPC-QVCO architecture contributes no voltages induction across M_{N1}-M_{N4} since the drain node of M_{C1}-M_{C4} are directly connected to GND, thus relaxing the $1/f$ up-conversion.

The quadrature generation is obtained through coupling of two identical oscillators in such a way that forces their outputs to oscillate 90° out of phase, with a tradeoff of two times in area and power utilization of a single LC oscillator [4].

SIMULATION RESULTS

Figure 6 illustrates the inductance and quality factor variation of the designed stacked spiral inductor extracted utilizing ASITIC tool. The designed inductor consumes an area of 100x100μm^2 with 3.25 number of spiral turns. From Figure 6 it is evident that the inductance variation is somewhat constant with frequency. At frequency well below the peak in the inductor Q, the shunt parasitic of the spiral inductor has little effect and consequently the inductive reactance and Q factor increases with frequency. However as the operating frequency continues to rise, the energy dissipation in the semiconducting substrate and the ac resistance of the metallization begins to increase faster than the inductive reactance, thus the Q factor peaks and then decreases.

Figure 7 describes the tuning characteristic of the designed pMOS based capacitor. From Figure 7, when the diffusion voltage is constant and the dc voltage applied at the gate V_{CTRL}, is increased the MOS capacitor varies from the inversion region to the accumulation region of operation. The simulated varactor consists of 130 segments with a total gate dimension of 650μm x 0.18μm. The size of each segment is 5μm x 0.18μm.

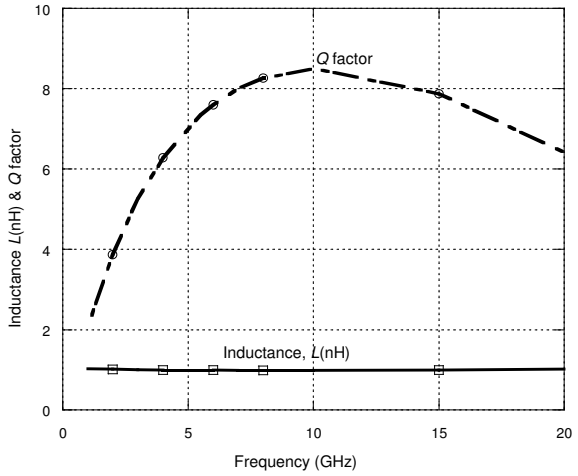

Fig. 6: Inductance L and Q factor characteristic

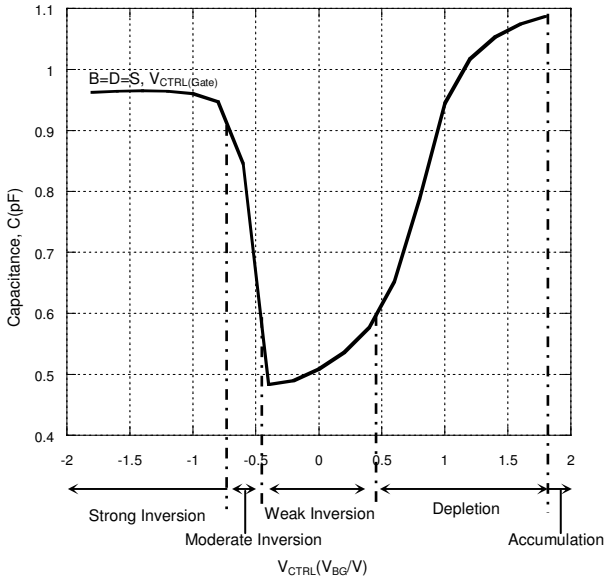

Fig. 7: Tuning characteristic for pMOS based capacitor with B=D=S

Figure 8 describes the pre-layout phase noise performance of the designed pMOS based SIPC-QVCO in comparison with conventional LC-QVCO topology. It is observed that the SIPC-QVCO has superior close in phase noise suppression. Figure 9 describes the pre-layout tuning characteristic of the designed QVCO. The tuning frequency ranges from approximately 3.2-3.6GHz.

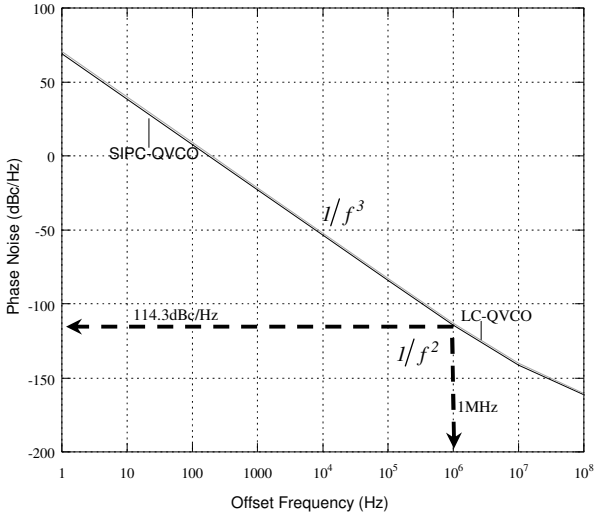

Fig. 8: Simulated phase noise versus offset frequency at 3.5GHz.

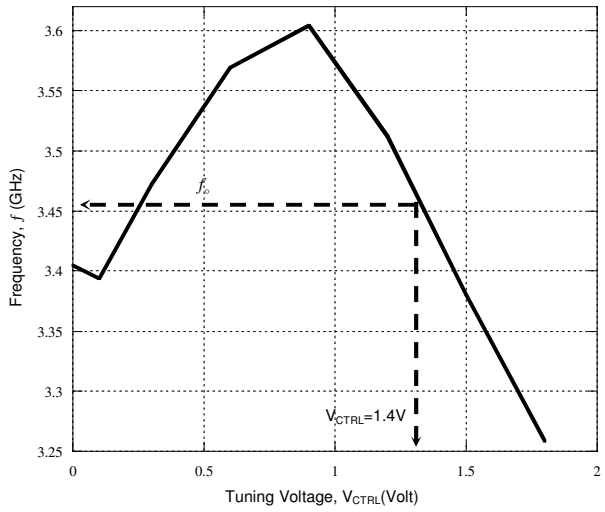

Fig. 9: Tuning characteristic of the complementary SIPC-QVCO

Figure 10 illustrates the physical implementation of the complementary SIPC- QVCO, implemented in 0.18µm CMOS technology and consumes a dimension of 1.9x1.16mm^2. The layout focuses on the symmetry of the balanced circuit.

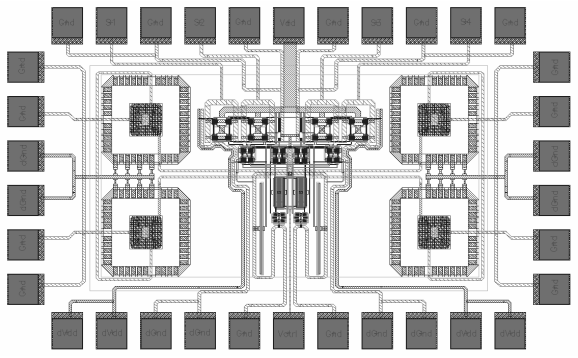

Fig. 10: Complementary SIPC-QVCO physical layout

Table I summarizes the simulated performance of the fully integrated complementary SIPC-QVCO.

Table I: Complementary SIPC-QVCO performance summary

Parameter	Result
Supply Voltage	1.8-V
Tuning Range	400-MHz
Tuning Voltage	0.9~1.8-V
$f_\circ$	3.45-GHz
Phase Noise	-114.3 dBc/Hz @ 1MHz
Power Dissipation	
QVCO Core	11mW
Open Drain Buffer	115mW

CONCLUSION

A low phase noise differential complementary based SIPC QVCO in comparison of the conventional LC-QVCO architecture is presented in compliance with IEEE 802.11a two step up-conversion outlines. An investigation of the stacked spiral inductor and pMOS varactor is performed in optimizing the design of the realized QVCO architecture.

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