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Study the Characteristic of P-Type Junction-Less Side Gate Silicon Nanowire Transistor Fabricated by Atomic Force Microscopy Lithography

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Abstract: Problem statement: Nanotransistor now is one of the most promising fields in nanoelectronic in order to less energy consuming and application to create developed programmable information processors. Most of Computing and communications companies invest hundreds of millions of dollars in research funds every year to develop smaller transistors. **Approach:** The Junction-less side gate silicon Nano-wire transistor has been fabricated by Atomic Force Microscopy (AFM) and wet etching on p-type Silicon On Insulator (SOI) wafer. Then, we checked the characteristic and conductance trend in this device regarding to semi-classical approach by Semiconductor Probe Analyser (SPA). **Results:** We observe in characteristic of the device directly proportionality of the negative gate voltage and Source-Drain current. In semi classical approach, negative Gate voltage falling down the energy States of the Nano-wire between the source and the drain. The graph for positive gate voltage plotted as well to check. In other hand, the conductance will be following characteristic due to varying the gate voltage under the different drain-source voltage. **Conclusion:** The channel energy states are supposed to locate between two electrochemical potentials of the contacts in order to transform the charge. For the p-type channel the transform of the carriers is located in valence band and changing the positive or negative gate voltage, make the valence band energy states out of or in the area between the electrochemical potentials of the contacts causing the current reduced or increased.

Key words: Silicon Nanowire Transistor (SNWT), Density of State (DoS), electrochemical potential

INTRODUCTION

In last decade, interest in Nano-Wire (NW's) had dramatically increased regarding to down scaling in semiconductor device technology. Working in nanoscale is very sensitive and tricky in order to a lot of necessary information are still unknown about it. Nano-wire transistor channel lengths continue to shrink rapidly and new ways for improving of the nanowire transistor have been investigated (Timp *et al*., 1999; Lee *et al*., 2001; Cheng *et al*., 2001; Rim *et al*., 1998) and the high mobility channel materials (Leitz *et al*., 2001; Yeo *et al*., 2002; Moezi *et al*., 2008). In this work we try to explain the characteristic Nano-scale transistors and seeking for explaining the SNWT device base on semiclassical approach or at least near-ballistic operation. First we express the fabrication method base on the AFM lithography and etching, .then plot the I_V graphs.

The operation of the MOSFET's and other nanowire transistors in semiclassical or ballistic regime has been explained by analytical models (Javey *et al*., 2002; Datta *et al*., 1998; Abdul-Rahman and Wang, 2010) and some numerical simulations (Assad *et al*., 2000; Ren *et al*., 2003).

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First we try to express the device and its structure fabricated by AFM scanning probe microscopy on SOI substrate. Finally, base on the previous publication about the silicon nanowire transistor and considering to the unique structure and characteristic of the device, try to explain the behaviour by the ballistic and semi-ballistic approach (Natori, 1994; 2001; Hashim and Rasmi, 2006; Maiti and Maiti, 2010).

MATERIALS AND METHODS

The nanometer-scaled electronic design pattern was fabricated on (100) silicon on insulator wafer by using Scanning Probe Microscopy (SPM) via Atomic Force Microscope (AFM) nanolithography process. In this work we make a nano-electronic device fabrication process based on KOH etch applied to structures defined by AFM nanolithography. The samples with a surface area 1-1.5 cm2 were cut from p-type Silicon On Insulator (SOI) <111> wafers phosphorus doped, resistivity 5-10 Ωm, diameter 100±0.5mm, thickness 525 ± 25 μm (Fig. 1). The SOI were used was as-grown and not subjected to any heat treatment. The samples were cleaned by using NH4OH CMOS grad and H_2O_2 heated at 80°C for 15 minutes to remove the organic contaminants, followed by rinsing with De Ionized Water (DIW). Solution from HCl and H_2O_2 were used to clean the ion metal on surface and heated at 80°C for 15 minutes, followed by DIW. Diluted HF, ratio 1:20 were use to remove the native oxide layer on SOI (Abdullah *et al*., 2010; Lew and Sabar, 2010).

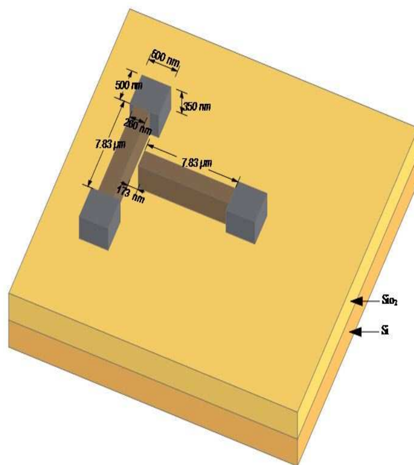

Fig. 1: Sketch of the nano-wire transistor fabricated by AFM nanolithography (Abdullah *et al*., 2010; Lew and Sabar, 2010)

All samples were cleaned with HF to give all samples the same starting conditions. After cleaning, the sample were place in the beaker, containing the aqueous KOH (Merck, p.a) varies in concentrations from 10% wt. to 40% wt. All the samples were etched in that solution for 12 sec in 60°C with and accuracy ±5°C. The nanometer-scaled electronic structure of the transistor is prepared by using of the-AFM nanolithography, which set up with constantly AFM mood in all necessary parameters. The pattern is formed on Silicon-On-Insulator (SOI) <100>. Before growth oxide as a mask (desired pattern), the SOI (substrate) were followed cleaning procedure as above mentioned. Then the sample was designed the simple transistor pattern as in Fig. 2 and 3.

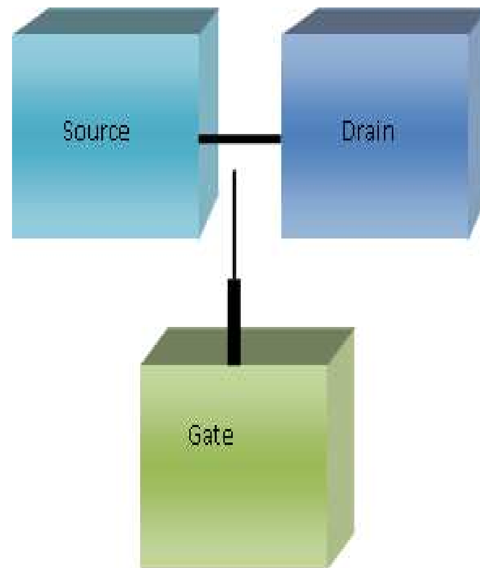

Fig. 2: Simple transistor pattern design by using AFM nanolithography

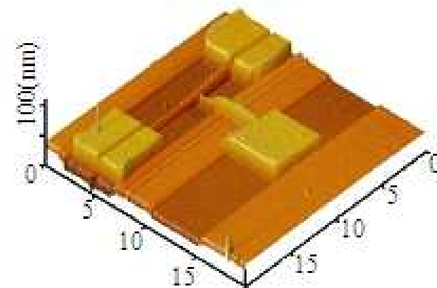

Fig. 3: Simple transistor pattern on SOI after etched with 10% wt. KOH + 10% vol. IPA (Abdullah *et al*., 2010; Lew and Sabar, 2010)

RESULTS

The characteristic graph of the device with both negative and positive voltage been measured. In Fig. 4 we can observe the behaviour of the conventional transistors for negative gate voltage applied. On the other hand, as we can see in Fig. 5 applying the positive voltage on the gate reduces the current. For the conductance as well, the graph plotted in Fig. 6 demonstrate the obvious dependence of the gate voltage for the conductance.

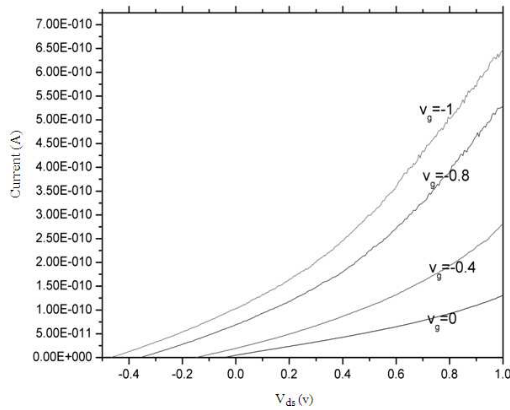

Fig. 4: Characteristic for the nano-wire transistor for negative gate voltage

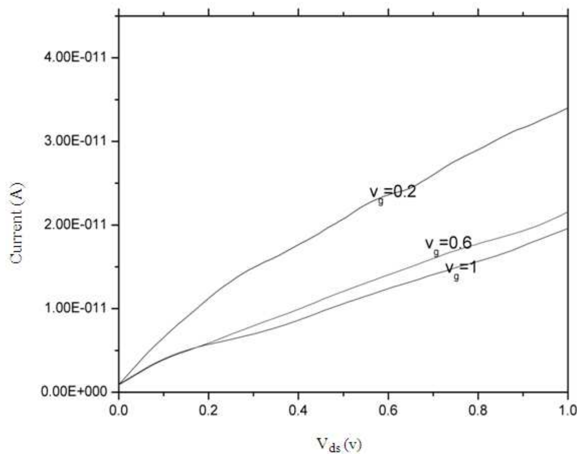

Fig. 5: Characteristic for the nano-wire transistor for positive gate voltage (Abdullah *et al*., 2010)

DISCUSSION

Consider to the device structure which consist of the source (left contact), channel (Si nanowire) and drain (right contact). After coupling of the source and drain and channel to each other electrons flow in and out bring the device all in equilibrium with a common electrochemical potential, μ, just like the material in equilibrium in temperature T. The average number of electrons in any energy level is given by Fermi function Eq. 1:

$$f_0(E-\mu) = \frac{1}{1+\exp\frac{E-\mu}{k_B T}} \qquad (1)$$

Which:

μ = The electrochemical potential (under some condition we can imply it as the fermi level)

k_B = The Boltzman constant

As it is showing in 'Fig. 4' for ballistic device, with $\mu_1 = E_{F1}$, $\mu_2 = E_{F2}$, we can see the array of the states and levels. We know under equilibrium condition the Fermi function gives us the total energy.

As a matter of fact, applying the battery voltage, V_D, lowers the energy levels in drain contact compare to the source contact (assuming V_D is positive) and keep them as the electrochemical potentials separated by qV_D (Datta, 2005) Eq. 2:

$$\mu_1 - \mu_2 = qV_D \qquad (2)$$

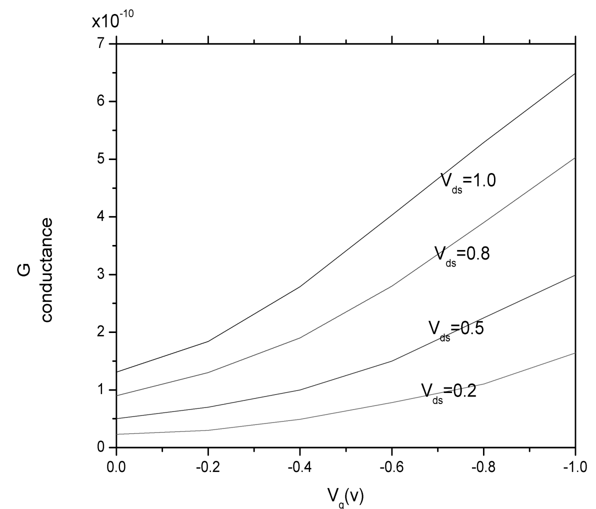

Fig. 6: Conductance Vs gate voltage under different drain-source voltage

This difference in electrochemical potential is giving rise two different fermi function and accordingly each contact seeks to bring the channel into equilibrium. Source injects the flux of carriers into the device some carriers reflected in order to potential barriers within the device and the rest pass through the channel toward the drain (Ren *et al*., 2003; Datta, 2005). We treat the carriers as the semiclassical particles and the Boltzman equation for finding the distribution function f ($\bar{r}$, $\bar{k}$, t) should be considered.

In order to Ballistic transforming, electron density is Eq. 3:

$$n(x) = \int dE[LDOS_L(x,E)f_L(E) + LDOS_R(x,E)f_R(E)] \quad (3)$$

Which L and R refer to the left and right contacts of the device and LDOS is the local density of states. The current flowing from source to drain (drain to source) will obtained simply by timing the transmission probability T(E) with Fermi function and net current would be (Datta, 1997) Eq. 4:

$$I = \frac{e}{h^2}\int dET(E)[f_L(E) - f_R(E)] \quad (4)$$

In this equation the difference of Fermi level and Fermi function between the source and drain is driving term for the net current.

The average number of electron N in channel steady state will be something intermediate between $f_1(\varepsilon)$ and $f_2(\varepsilon)$. For left and right contact the net flux I_1, I_2 would be as follows Eq. 5-6:

$$I_1 = \frac{q\gamma_1}{h}(f_{1(\varepsilon)} - N) \quad (5)$$

$$I_2 = \frac{q\gamma_2}{h}(f_{2(\varepsilon)} - N) \quad (6)$$

Which γ_1 and γ_2 are the broadening function or straightforwardly we can say $\frac{\gamma_1}{h}$ and $\frac{\gamma_2}{h}$ are the rates at which an electron located in energy level ε would scape from the source or through the drain respectively. Actually γ is proportional to mean free path λ. By using some approximation for steady level we can write (Datta, 2005) Eq. 7:

$$I = \frac{q\gamma_1\gamma_2}{h\gamma_1 + \gamma_2}(f_{1(\varepsilon)} - f_{2(\varepsilon)}) \quad (7)$$

To integrate over the distribution states, $D_\varepsilon(E)$ dE Eq. 8:

$$I = \int_{-\infty}^{+\infty} dED_\varepsilon(E)\frac{q\gamma}{2h}(f_{1(E)} - f_{2(E)}) \quad (8)$$

Which we assume that:

$$\frac{\gamma}{2} = \frac{\gamma_1\,\gamma_2}{\gamma_1 + \gamma_2}$$

Source contact try to fill the available states inside the channel and hold the state in $f_{1(E)}$, meanwhile drain try to empty them out holding the condition in $f_{2(E)}$. If for any reason the states numbers or location change then it will affect the net current of the device. Gate voltage by changing energy states condition inside the channel always affect the current (except for the off- line current). In order to applying negative or positive gate voltage the states will slide down or up between Fermi energy (electrochemical energy level) respectively. We can clearly see in both "(7)" and "(8)" equation that the driving term in current equation is the energy level between Fermi interval of source and drain ($f_{1(E)} - f_{2(E)}$) and for the energy states in channel between this interval the current will exist.

The density of electron and conductance G = I/V will obtained as (Datta, 2005) Eq. 9-10:

$$N = \int dED(E-U)\frac{f_1\gamma_1 - f_2\gamma_2}{\gamma_1 + \gamma_2} \quad (9)$$

$$G = q^2\int d(E-U)\frac{\gamma}{2h}\frac{f(\varepsilon)(1-\int(\varepsilon))}{k_{BT}} \quad (10)$$

Quantity U is the self consistent potential extracted by the simultaneous solving of the Poisson-Schrodinger equation. In fact, U has a very important role in finding any quantity of the device depends on the free and induced charge in channel.

CONCLUSION

As long as the substrate is p-type the major carriers are the holes. Since conduction in the channel depends on availability of states around electrochemical potential μ and not the total number of electron, consequently, the amount of current will be measured by existence or density of the energy states as mentioned previously.

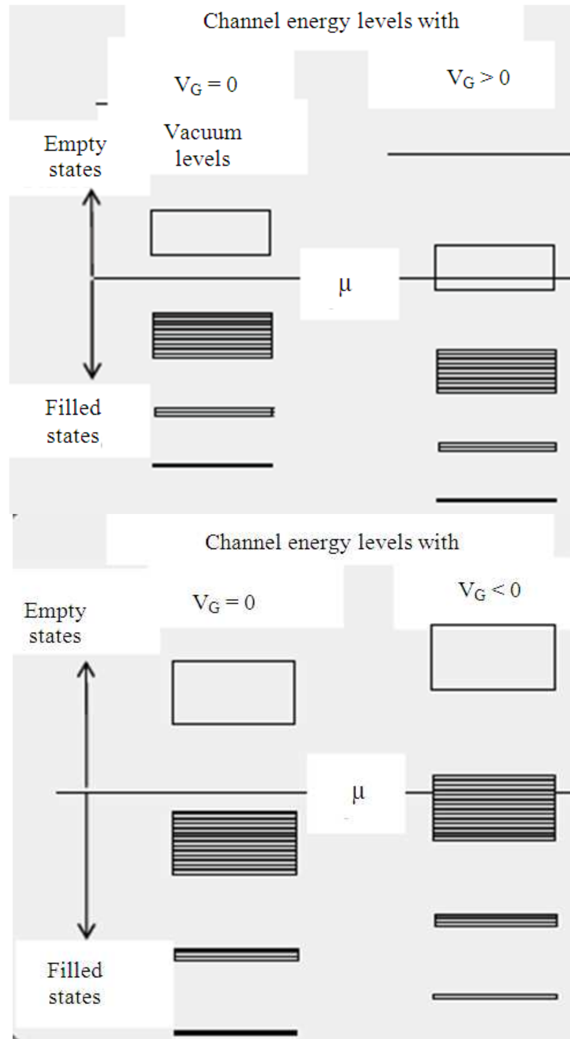

Fig. 7: Fermi energy (or electrochemical potential) is held fixed by source and drain reservoirs. Apply a positive and negative gate voltage and band energy levels move down and upward respectively (Datta, 2005)

The negative gate voltage decreases the number of electrons in the channel nevertheless the channel become more conductive because the negative voltage pull the states up around the Fermi level difference ($f_{1(E)}$-$f_{2(E)}$) and electrochemical level therefore, the graph shows increasing in current by increasing the gate voltage which is predicted by ballistic transformation model. In 'Fig. 4' we can see the characteristic graph for the device under negative gate voltage. In fact, the valance band located between the electrochemical levels of the source and drain, has the important role in charge transportation.

The energy states between the source and drain located in channel slide up by negative gate voltage and driving the energy state between the source and drain area (LDOS L-LDOS R) upward (Fig. 7). This phenomenon increases the number of available states, as the result the current will raise as we can see in the graph under influence of raising the gate voltage. Applying the positive gate voltage make the net current decreased. The fact is, increasing the gate voltage drive the Density Of States (DOS) out of the (μ_1-μ_2) area by sliding down the states. Accordingly we can see particular decline in amount of the current. In other hand, it is clearly inferred from the conductance (G) graph (Fig. 6) that the device follows the semi-classic transforming. We can see how the conductance varied with the gate voltage under different drain-source voltage. Gate threshold voltage appeared to be in 0.2V and by raising the voltage the conductance and accordingly the N will increased.

REFERENCES

Abdullah, A.M., S.D. Hutagalung and Z. Lockman, 2010. Etching effect on the formation of silicon nanowire transistor patterned by AFM lithography. Proceedings of the International Conference on Nanotechnology: Fundamentals and Applications, Aug. 4-6, International ASET, Ottawa, Ontario, Canada, pp: 1-7.

Abdul-Rahman, H. and C. Wang, 2010. Critical retrospect on conventional and luminescent solar concentration devices, Am. J. Environ. Sci., 6: 428-437. DOI: 10.3844/ajessp.2010.428.437

Assad, F., Z. Ren, D. Vasileska, S. Datta and M. Lundstrom, 2000. On the performance limits for Si MOSFETs: A theoretical study. Elect. Devices, IEEE Trans., 47: 232-240. DOI: 10.1109/16.817590

Cheng, Z.Y., M.T. Currie, C.W. Leitz, G. Taraschi and E.A. Fitzgerald *et al*., 2001. Electron mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-On-Insulator (SGOI) substrates. Elect. Device Lett., IEEE, 22: 321-323. DOI: 10.1109/55.930678

Datta, S., 1997. Electronic Transport in Mesoscopic Systems. 1st Edn., Cambridge University Press, ISBN: 10: 0521599431, pp: 377.

Datta, S., 2005. Quantum Transport: Atom to Transistor. 2nd Edn., Cambridge University Press, ISBN: 10: 0521631459, pp: 418.

Datta, S., F. Assad and M.S. Lundstrom, 1998. The silicon MOSFET from a transmission viewpoint. Superlattices Microstructures, 23: 771-780. DOI: 10.1006/SPMI.1997.0563

Hashim, U. and A. Rasmi, 2006. Single-Electron Transistor (SET) process and device simulation using SYSNOPSYS TCAD tools. Am. J. Applied Sci., 3: 1933-1938. DOI: 10.3844/ajassp.2006.1933.1938

Javey, A., H. Kim, M. Brink, Q. Wang and A. Ural *et al*., 2002. High-K dielectrics for advanced carbon-nanotube transistors and logic gates. Nature Mater., 1: 241-246. DOI: 10.1038/nmat769

Lee, M.L., C.W. Leitz, Z. Cheng, A.J. Pitera and T. Langdo *et al*., 2001. Strained Ge channel p-type metal-oxide-semiconductor field-effect transistors grown on $Si_{1-x}Ge_x/Si$ virtual substrates. Applied Phys. Lett., 79: 3344-3346. DOI: 10.1063/1.1417515

Leitz, C.W., M.T. Currie, M.L. Lee, Z.Y. Cheng and D.A. Antoniadis *et al*., 2001. Hole mobility enhancements in strained $Si/Si_{1-y}Ge_y$ p-type metal-oxide-semiconductor field-effect transistors grown on relaxed $Si_{1-x}Ge_x$ ($x<y$) virtual substrates. Applied Phys. Lett., 79: 42-46. DOI: 10.1063/1.1423774

Lew, K.C. and D.H. Sabar, 2010. Silicon nanowire transistor fabricated by AFM nanolithography followed by wet chemical etching process. Int. J. Nanosci., 9: 289-293. DOI: 10.1142/S0219581X1000682X

Maiti, T.K. and C.K. Maiti, 2010. DFM of strained-engineered MOSFETs using technology CAD. Am. J. Eng. Applied Sci., 3: 683-692. DOI: 10.3844/ajeassp.2010.683.692

Moezi, N., D. Dideban and A. Ketabi, 2008. A novel integrated SET based inverter for nano power electronic applications. Am. J. Eng. Applied Sci., 1: 219-222. DOI: 10.3844/ajeassp.2008.219.222

Natori, K., 2001. Scaling limit of the MOS Transistor--A ballistic MOSFET. IEICE Trans. Elect., 84: 1029-1036.

Natori, K., 1994. Ballistic metal-oxide-semiconductor field effect transistor. J. Applied Phys., 76: 4879-4890. DOI: 10.1063/1.357263

Ren, Z., R. Venugopal, S. Goasguen, S. Datta and M.S. Lundstrom, 2003. NanoMOS 2.0: A two-dimensional simulator for quantum transport in double-gate MOSFETs. Elect. Devices, IEEE Trans., 50: 1914-1925. DOI: 10.1109/TED.2003.816524

Rim, K., J.L. Hoyt and J.F. Gibbons, 1998. Transconductance enhancement in deep submicron strained Si n-MOSFETs. Proceedings of the International Electron Devices Meeting, Technical Digest, Dec. 6-9, IEEE Xplore Press, San Francisco, CA, USA., pp: 707-710. DOI: 10.1109/IEDM.1998.746455

Timp, G., J. Bude, K.K. Bourdelle, J. Garno and A. Ghetti *et al*., 1999. The ballistic nano-transistor. Proceedings of the International Electron Devices Meeting, Technical Digest, Dec. 05-08, IEEE Xplore Press, Washington, DC, USA., pp: 55-58. DOI: 10.1109/IEDM.1999.823845

Yeo, Y.C., V. Subramanian, J. Kedzierski, P. Xuan and T.J. King *et al*., 2002. Design and fabrication of 50-nm thin-body p-MOSFETs with a SiGe heterostructure channel. Elect. Devices, IEEE Trans., 49: 279-286. DOI: 10.1109/16.981218