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Source Couple Logic (SCL): Theory and Physical Design

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Abstract: This study describes and presents the analysis for the Source-Coupled Logic (SCL) inverter as will as the effect of submicron layout parasitics. The SCL inverter circuit model and its operation is defined. The analysis for the SCL is carried from the point of view of input/output voltage characteristics and the effect of noise margin. The inverter gate delay model is described and the effect of biasing current on the delay is shown. The result shows that, the delay of the SCL inverter is decreased as biasing current increase. The simulation is done based on the 0.18 μ Silterra PDK. Different layouts for SCL inverter have been investigated for its effect on output voltage swing, switching noise and the area. The results show an important effect on the SCL output signals. Post-Simulation was carried out on all proposed layouts using HSPICE and using 0.35 μ MIMOS Berhad PDK. The layout was done using Virtuous from Cadence where as the extraction done using Mentor Graphic-Caliber Interactive tool.

Key Words: Source Couple Logic (SCL), CMOS layout, RC parasitic in layout, analog circuit layout

INTRODUCTION

In the recent era, the interesting for high-speed high-resolution mixed-signal ICs has been growing due to the diffusion of applications based on digital signal processing, including audio and video signal processing, as well as over sampled sigma-delta Analog-Digital (A/D) and Digital-Analog (D/A) conversion[1-5]. In these ICs, analog and digital circuits are implemented on the same silicon substrate and the resolution of the analog circuitry is severely restricted by the amount of switching noise generated by the digital blocks[6-8]. Actually, due to the supply current spikes during switching, logic gates generate the power-supply switching noise[3,7,8-11], that couples with the analog circuits through supply lines and substrate coupling, thus degrading circuit resolution. In particular, the traditional CMOS static logic generates a high amount of noise and is thus not suitable for high-resolution applications. For instance, in[3], digital and analog blocks were implemented in two different chips to obtain the required resolution, even using analog circuits with a high noise rejection and exploiting techniques such as diffusion of guard bands, keeping separate analog and digital supply lines, pads and wires[6]. As a consequence, alternative logic styles with reduced supply current spikes during switching are needed to reduce the amount of switching noise. To avoid the degradation of resolution in mixed-signal ICs, a number of approaches have been proposed at different design levels of abstraction, from technology to the system level[6,9,12-13]. At the circuit level, the standard CMOS logic is not a feasible approach when a high resolution is required and a different logic style with reduced switching noise is required[3,6,14]. Among the possible topologies[6,12,13,15–23], one of the most successful logic styles is the Source-Coupled Logic (SCL)[6,15,17,20,23-26], which is based on the source-coupled pair of NMOS transistors and permits switching noise reduction by two orders of magnitude compared to standard CMOS logic[15,17].

In general, compared to CMOS static logic, SCL logic style allows switching noise to be reduced by two orders of magnitude[15,17]. Since the low switching noise feature of SCL is obtained at the cost of static power dissipation, a design methodology of SCL gates is required to meet specifications, while keeping power consumption as low as possible. Moreover, design criteria to intentionally manage the power-delay tradeoff are required.

SCL gates are differential. The implementation of logic functions is based on the series-gating approach, i.e., by stacking source coupled pairs[17,24,27-29]. However, this approach severely limits the minimum supply voltage allowed for proper operation of stacked transistor pairs, which can be a serious drawback in

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current low-voltage low-power circuits. Moreover, implementation of NAND/NOR functions often requires the use of multiple cascaded gates, since each gate has a fan-in limited to 2 or 3 for practical values of the supply voltage[17, 30-31], thus increasing the overall power consumption with respect to the case of a single gate.

In this study, the design procedure of SCL will be investigated and characterized. The SCL circuit topology and operation are explained. The SCL characterization, delay model and analytic model of noise margin is discussed and based on simulation, it is different characteristics are shown. Physical design and layout of SCL is considered for the effect of different layouts on SCL performance and amount of parasitics introduced as well as the noise effect. The simulation results of physical design are based on the post simulation using MIMOS Berhad PDK.

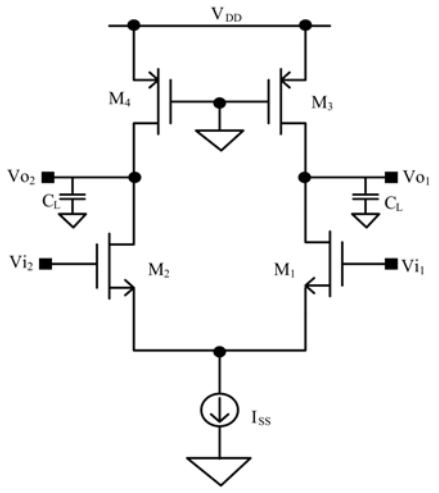

Fig. 1. SCL inverter

Topology and operation: SCL is a dual rail logic circuit that use both the variable and its complement (A, $\bar{A}$) as an input pair. The output of a dual rail circuit is also a pair (E, $\bar{E}$) that drives the next gate(s) in the logic cascade. However, dual rail logic interprets the difference (E-$\bar{E}$) as the logic variable instead of just one or the other. When viewed at the level of Boolean algebra, the use of both the variable and it is complement is superfluous; the result is the same as that found using a single-rail circuit. Moreover, dual rail networks are more complicated to wire[32].

The circuit schematic of SCL inverter gate, shown in Fig. 1, is made up of an NMOS source-coupled pair having transistors working in the saturation or cut off region, that approximate well the behavior of a voltage-controlled current switch. The biasing current (I_{ss}) is steered to one of the two output branches and converted into a differential output voltage by two PMOS transistor working in the linear region (Active load pull-up resistance)[26]. The logic function of the SCL is implemented by the logic block connected between the active load (PMOS) and the current source (I_{ss}). For an inverter/buffer, the logic block is the differential pair constructed by NMOS transistors M_1 and M_2[33].

The SCL gate uses PMOS active load, but other types of load, such as physical resistor or a diode-connected NMOS/PMOS could be used. However, resistor load is not normally chosen since large silicon area needed and its parasitic capacitance can be high. For the second type of load, the output levels will loss the threshold voltage furthermore; the MOS diode load is slower than the PMOS active load for practical bias currents[34].

The operation of the SCL logic is based on the input differential pair circuit. The two inputs control the flow of current through the two branches of the differential pair. For example, if V_{GS} (M_2) is higher than V_{GS} (M_1), the current I_{D2} exceeds the current I_{D1}. Therefore, the output voltage V_{o2} begins to drop until it reach steady sate , where the current going through PMOS active load (M_4) matches the I_{D2}. In mean time V_{o1} is charged to V_{DD} through M_3.

The output voltage swing V_{swing} is defined as voltage difference between V_{o1} and V_{o2} at steady state. The amount of current passing through the ON branch (M_2) controls the delay of the logic gate transition ($1\rightarrow0$), while the PMOS active load (M_3) controls the charging of the output nodes ($0\rightarrow1$ transition). Defining ΔV as the voltage drop of $M_3(M_4)$ due to the drain current equal to I_{ss}, the logic swing of the gate, V_{swing} equal $2\Delta V$. To achieve best performance , all current must pass through the ON branch and the load resistance (PMOS) should be small in order to reduce the RC delay. This guarantees that the voltage is V_{DD} - $I_{ss}.R_D$, where I_{ss} is the current flowing through current source and R_D is the PMOS equivalent linear resistance[33].

SCL Characteristics:

Input-Output transfer voltage: As conversion from current-to-voltage in the SCL inverter is performed by the two PMOS transistors M_3-M_4, both of which have a source-gate voltage equal to V_{DD} and a much smaller source-drain voltage (in order of hundred milivolts). Therefore, transistors M_3-M_4 work in the triode region and can be modeled as an equivalent linear resistor R_D[34].

Using the standard BSIM3v3 MOSFET model[35], under the static condition, PMOS transistor can be suitably approximated by an equivalent linear resistance R_D given by:

$$R_D \frac{R_{int}}{1-\frac{R_{DS}}{R\,int}} \quad (1)$$

where $R_{DS} = (R_{DSW}.1e\text{-}6)/W_p$ models the source/drain parasitic resistance which depends on the empiric model parameter R_{DSW} as well as the PMOS transistor effective channel width W_p. R_{int} is given by:

$$R_{int} = \left[\mu_{eff,p} C_{ox} \frac{W_p}{L_p}(V_{dd} - |V_{th,p}|)\right]^{-1} \quad (2)$$

This represent the intrinsic resistance of PMOS transistor in the linear region (it does not account for the parasitic drain/source resistance). In Eq. 2 the $\mu_{eff,p}$ represents the effective hole mobility, parameter L_p is the PMOS effective channel length, C_{ox} is the oxide capacitance per area and $V_{th,p}$ is the threshold voltage[26].

The output voltage $V_o(V_i)$ SCL inverter can be evaluated by substituting the equivalent resistance R_D in 1.

Thus, the differential output voltage V_o is equal

$$V_o = V_{o1} - V_{o2} = -R_D (i_{D1} - i_{D2}) \quad (3)$$

The minimum differential input (V_i) required to fully switch the entire tail current I_{ss} to one side is give by[36]:

$$I_{ss} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_i^2 \rightarrow V_i \sqrt{\frac{2I_{ss}}{\mu_n C_{ox}\frac{W}{L}}} \quad (4)$$

Which gives output transfer characteristics:

$$v_o(v_i) = \begin{cases} R_D I_{SS} & \text{if } v_i < -\sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W_n/L_n}} \\ -vR_D I_{SS}\sqrt{\frac{\frac{\mu_{eff,n}C_{ox}}{I_{SS}}\frac{W_n}{L_n}}{\left(\frac{\mu_{eff,n}C_{ox}}{I_{SS}}\frac{W_n}{L_n}v_i\right)^2}} & \text{if } |v_i| \le \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W_n/L_n}} \\ -R_D I_{SS} & \text{if } v_i > \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W_n/L_n}} \end{cases} \quad (5)$$

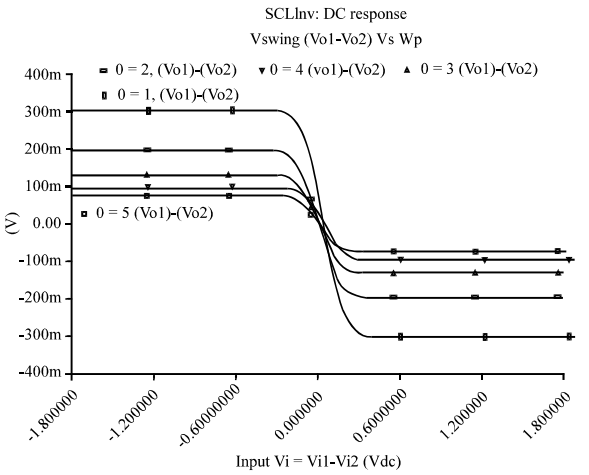

Fig. 2: Differential output voltage varying with the aspect ration of PMOS

Where, $V_i = V_{i1} - V_{i2}$ (Differential input). From 5, $V_{OL} = -R_D I_{ss}$ and $V_{OH} = R_D I_{ss}$, then the logic swing is equal to[34]:

$$V_{swing} = V_{OH} - V_{OL} = 2 R_D I_{ss} = 2 \Delta V \quad (6)$$

From 5, that output voltage swing (V_{swing}) is a function of R_D for fixed I_{ss}. R_D is controlled by the aspect ratio of PMOS, so for desired V_{swing}, the aspect ratio can be varied accordingly.

To verify the theoretical analysis, the simulation was carried out on the SCL inverter gate. For evaluate the V_{swing}, DC simulation is done by varying the aspect ratio of the PMOS with fixed I_{ss} =10μA.

Figure 2 shows the differential output voltage of SCL inverter as function of differential input (V_i) , when (V_i) is greater certain value the SCL inverter fully switch to either side and passing all I_{ss} to that side. The value of output voltage is function of R_D and it is controlled by the aspect ratio of PMOS.

The V_{swing} /2 ($I_{ss}.R_D$) must be kept low enough to ensure the NMOS transistors M_1-M_2 are not in the triode region. In particular, when the gate voltage of an NMOS transistor is high (equal to V_{DD}), the drain voltage is equal to V_{DD}- $I_{ss}.R_D$, the triode region can be avoided if the gate-drain voltage V_{GD} is lower than threshold voltage by:

$$V_{GD} = V_{DD} - [V_{DD} - R_D.I_{SS}] = R_D.I_{SS} \le V_{th,n} \quad (7)$$

Which imposes an upper bound to $I_{ss}.R_D$ and hence the logic swing as given by 6[34].

Noise Margin (NM): Due to the symmetrical property, the logic threshold is equal to zero ($V_{LT} = 0$) and the associated small-signal voltage gain is $g_{m,n}.R_D$, (where $g_{m,n}$ is the small-signal transconductance of transistor M1-M2 with $I_{D1,2} = I_{ss}/2$)[26].
Since $v_{i1} = v_{i2} = v_{o1} = v_{o2} = V_{DD} - \Delta V/2$ and $I_{D1,2} = I_{ss}/2$, when the gate is biased around logic threshold, voltage V_{DS} of transistor M1-M2 is equal to their V_{GS}. Hence, the resulting expression of the voltage gain A_V is[26]:

$$A_V = g_{m,n}R_D = \Delta V\sqrt{\mu_{eff,n}C_{ox}\frac{W_n}{L_n}\frac{1}{I_{ss}}} \quad (8)$$

The NM is equal to NM_L (for Low-Logic) and similar to NM_H (for High-Logic) due symmetrical property, which is defined as $NM_H = V_{OHmin} - V_{IHmin}$ ($NM_L = V_{ILmax} - V_{OLmax}$) where V_{ILmax} and V_{IHmin} are the input voltage values such that $\partial vo/\partial vi = -1$. V_{OLmax} and V_{OHmin} are the corresponding output voltages ($V_{OLmax} = Vo(V_{IHmin})$ and $V_{OHmin} = Vo(V_{ILmax})$)[34]. By differentiating (5) for v_i and setting it to -1, V_{IHmin} results is

$$V_{IH\,min}\sqrt{\frac{2I_{SS}}{\mu_{eff,n}C_{OX}\frac{W_n}{L_n}} - \frac{I_{SS}}{2\mu_{eff,n}C_{OX}\frac{W_n}{L_n}}\frac{1}{A_V^2}\left(\sqrt{1+8A_V^2}+1\right)}$$

$$V_{IH} \cong \sqrt{\frac{2I_{ss}}{\mu_{eff,n}C_{ox}\frac{W_n}{L_n}}}\left(1-\frac{1}{\sqrt{2A_V}}\right) \quad (9)$$

Where $A_V >> 1/\sqrt{8}$ has been assumed.

Approximating V_{OHmin} to $-\Delta V$ leads to the following expression of NM:

$$NM = \Delta V\left(1-\frac{\sqrt{2}}{A_V}\sqrt{1-\frac{1}{\sqrt{2A_V}}}\right) \cong \left(1-\frac{\sqrt{2}}{A_V}\right) \quad (10)$$

Where $A_V >> 1/\sqrt{2}$ was assumed. The value of NM is proportional to half the logic swing[34].

Simulations were performed by setting V_{swing} to 600 mV, I_{ss} to 10 uA and varying the NMOS aspect ratio (dimensions in nm). The effect of A_V is shown in Fig. 3, which shows how ∂vo/∂vi changes with W_n. A_V increases for low values of NMOS aspect ratio then asymptotically tends to a constant value as illustrated in Fig. 4. The SCL inverter gate output delay increases linearly as W_n increases thus limiting us to small W_n, as shown Fig. 5.

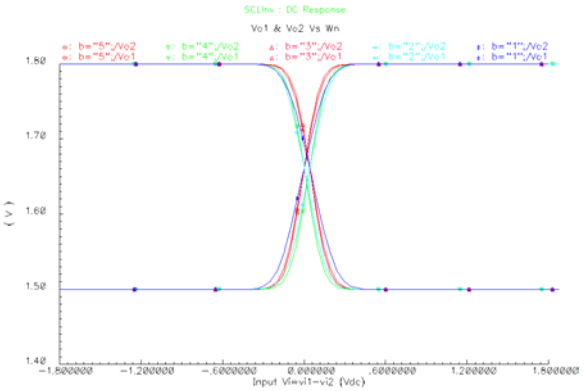

Fig. 3: Change of $\partial V_o/\partial V_i$ with different W_n

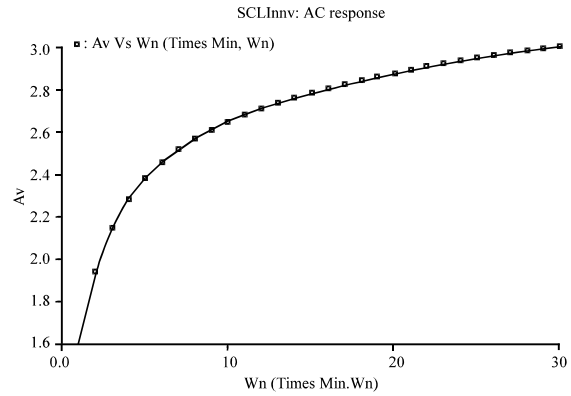

Fig. 4: A_V versus NMOS aspect ratio

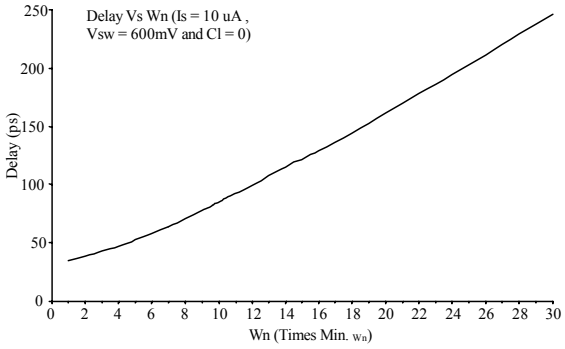

Fig. 5: SCL inverter delay versus W_n

Delay analysis: To model the propagation delay, $\tau_{PD,SCL}$, of the SCL inverter , it is useful to observe that NMOS transistors work in the saturation region most of the time and their source voltage is the same for both input logic values (it's fixed by the NMOS transistor in the on state). Thus, after linearization the circuit around the logic threshold $v_i = 0$, the half-circuit concept

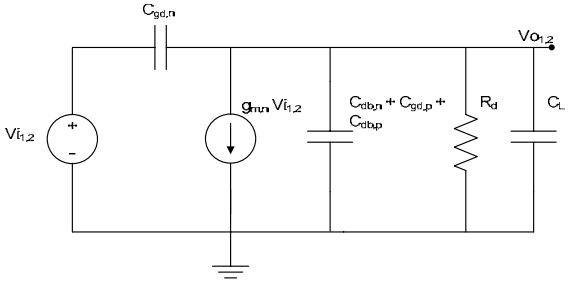

Fig. 6: Equivalent linear half-circuit of the SCL inverter

applies, since the circuit is symmetrical and it's input is differential[25].

Figure 6, shows the small-signal model of the half-circuit concept. The circuit has time constant (τ) that can be evaluated by applying the open-circuit time constant method[37]. It gives the resulting delay as 0.69τ, assuming a step input waveform and neglecting the high-frequency zero. Hence, the propagation delay $\tau_{PD,SCL}$ of the SCL gate is given by[34]:

$$\tau_{PD,SCL} = 0.69*R_D(C_{gd,n}+C_{db,n}+C_{gd,p}+C_{db,n}+C_L) \quad (11)$$

The NMOS capacitance $C_{gd,n}$, in (11) is evaluated in the saturation region. Thus its value equal to the overlap capacitance $C_{gd0}.W_{eff}$ between the gate and the drain. Junction capacitances $C_{db,n}$ and $C_{db,p}$ can be linearized by modifying their value in a zero-bias condition via coefficients K_j according to[39]. Capacitance $C_{gd,p}$ is equal to the sum of the overlap contribution $C_{gd0}W_{eff,p}$ and the intrinsic contribution associated with the channel charge of the PMOS transistors working in the linear region, $C_{gd,p,int}$. In particular, we can adopt the BSIM3v3 capacitance model[36], which express capacitance $C_{gd,p,int}$ as the derivative of charge flowing into drain Q_D with respect to the voltage V_D[25]:

$$C_{gd,p,int} = \frac{\partial Q_D}{\partial V_D} \cong \frac{3}{4} A_{bulk,max} WLC_{OX} \quad (12)$$

This derivation assumes the gate, source and bulk voltage are constant and using $A_{bulk,max}$ (maximum bulk charge effect) slightly greater than unity and assuming

$$V_{SD} << V_{SG} - |V_{th}|/A_{bulk}.$$

To validate the delay model, the bias current was varied from 10-100 μA, the transistor aspect ratios were sized to obtain the typical value V_{swing} = 600 mV, A_V = 1.94 and the load capacitance C_L was set to 0 F, 100 fF and 1 pF, respectively.

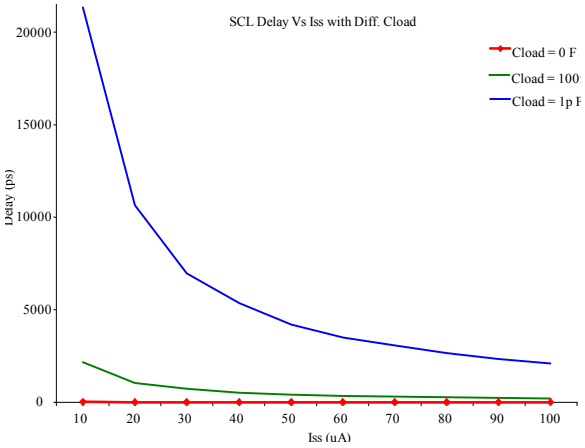

Fig. 7: Delay versus bias current I_{SS} with C_L= 0, 100 fF and 1pF respectively

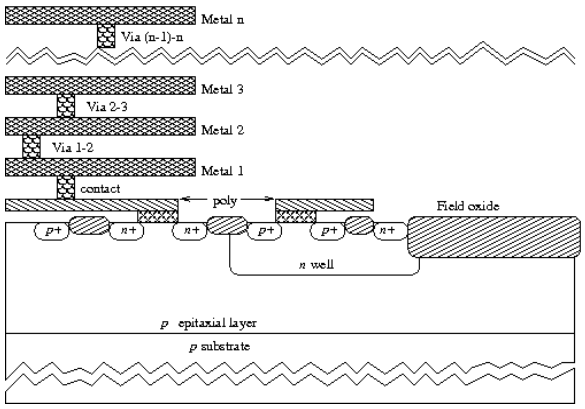

Fig. 8: Interconnection parastics capcitances among CMOS layers

Figure 7 show the results. As expected, the delay is decreased by increasing the bias current I_{ss} and asymptotically tends to a constant value.

SCL physical design: As the design margins decrease steadily, the analogue problems (matching, crosstalk) rises it is affect to the circuit's performance. The dominance of parasitics has shifted from the vertical plan (towards GND) to the lateral one (cross)-coupling. The electrical parasitic extraction is the process of estimating or calculating the undesirable by product elements of the physical layout of a circuit. It is utilized to improve the model behavior of a circuit and to highlight the design imperfections and allows the designer to make the circuit more robust. The electrical parasitics are the sum of the electrical characteristics (resistance, inductance and capacitance) of any interconnects (Fig. 8)[39].

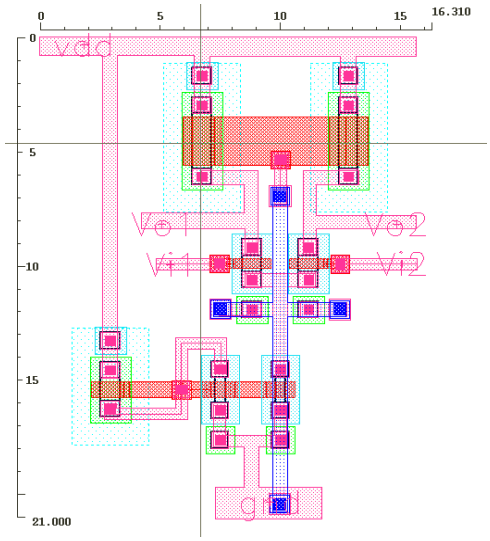

Fig. 9: 1st layout of SCL inverter

Those interconnects have an important contribution through their R and C components on the electrical circuit parameters such as delay, crosstalk or matching, especially in deep submicron technologies and that's why it becomes more important to take these effects into account during the IC simulations[40,41].

All mentioned parasitics are dependent on the way of laying out the circuit in the IC design; the way of laying out the circuit is the amount of RC parasitic is added, so, that is affecting all performance of the circuit. In the next sections different techniques of laying SCL inverter will be applied to examine the effect of RC parasitic on the output signals by employing post-simulation with input dual opposite pulses shown in Fig. 2, the limits and constrain of all layouts are the design rules of the MIMOS 0.35u PDK.

First layout: Direct layout is applied and each transistor is laid as discrete component according to layout design rule. Whole W and L of NMOS/PMOS transistors are laid directly. The signal paths among different interconnections terminals are made directly as short as possible with minimum path width. Two metal layers are used M1 and M2 for signal paths. This layout utilizes 14 S/D interconnections. This layout is shown in the Fig. 9.

Second layout: Fingering technique is applied to divide the W of NMOS and PMOS on two transistors connected in parallel as shown in the Fig. 10. This layout utilizes 17 S/D interconnections and two layers M1 and M2. This layout utilizes more area than first one due of fingering.

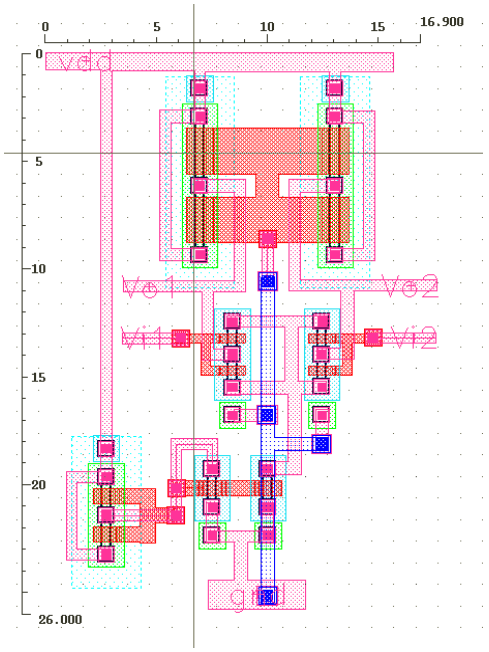

Fig. 10: 2nd layout of the SCL inverter

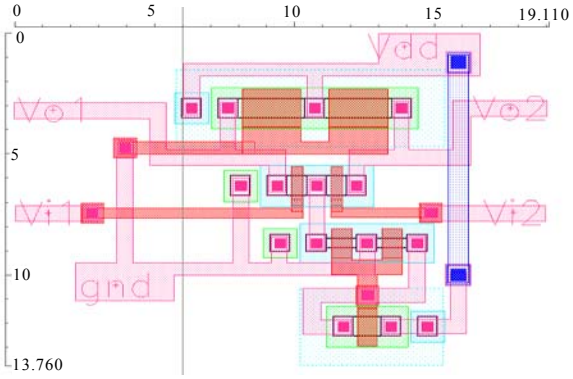

Fig. 11: Comb layout of SCL inverter

Third layout: Comb In this layout the NMOS and PMOS transistors are laid in comb way, which reduces the area and drain/source interconnections, also its provides interdigitized and common centroide structure as shown in Fig. 11. This layout utilizes 11 S/D interconnections.

Forth layout: Fingering and Comb Both, fingering and comb techniques are applied in this time as shown in Fig. 12 and 14 S/D interconnections are used. Comparing with third layout, area is increased.

Output results: SCL inverter laid out with four different arrangements to investigate the affect of result

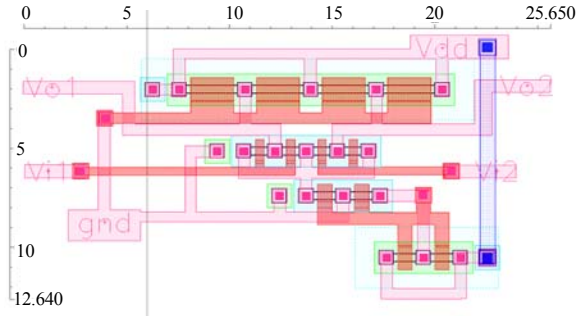

Fig. 12: Fingering and comb layout of SCL inverter

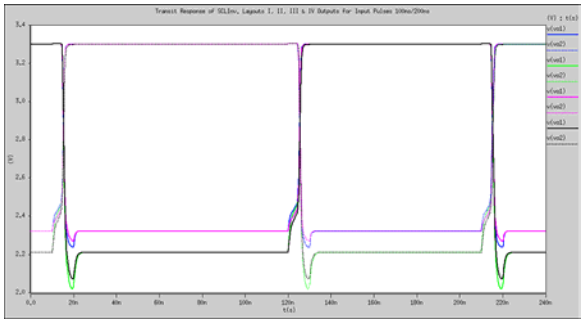

Fig. 13: Outputs of SCL inverter netlist and layouts for 100/200ns input pulses

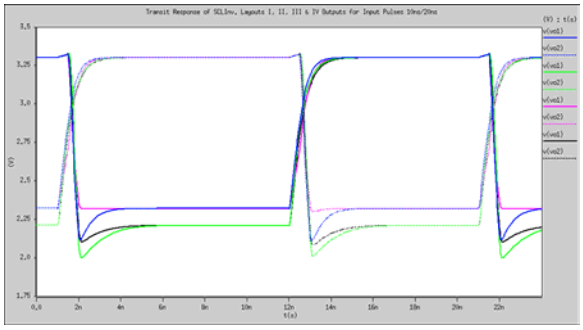

Fig. 14: Outputs of SCL inverter netlist and layouts for 10/20ns input pulses

RC parasitic on the performance of the SCL inverter. For same inputs, the result shows that the output V_{swing} of the 2nd and 4th SCL inverter layout is greater than 1st and 3rd due of more interconnections of drain and source by using fingering which cause more parasitic resistance. The parasitic capacitance in 2nd layout is more than in 4th layout as more S/D interconnections are used, so more areas, which clear from switching noises. Even, the 3rd layout introduces more parasitic capacitance than 1st for the same reason. All layouts introduce some amount of resistance due of paths and interconnections which increase the V_{swing} than netlist V_{swing}, Fig. 13, shows the outputs of SCL inverter net list and it is four layouts for input pulses of 100ns/200ns.

As the frequency of inputs pulses increases, the shape of output signals get distorted totally as the RC parasitic is function of signal frequency and the signal delay become superfluous Fig. 14.

CONCLUSION

The study work presents the basic theory and operation of SCL logic as well as the effect of layout on the SCL performance. The delay of inverter SCL gate is validated by Cadence-Spectre simulation using a 0.18µ Silterra PDK. Different parameters which affect the SCL logic are characterized. The SCL delay is decreased by increase of biasing current. The output voltage swing is small which reduce the dynamic power consumption. The SCL logic draws a fixed static current from the supply. The other advantages of SCL which inherited from its differential design include common mode noise rejection, insensitivity to process change and friendliness to neighboring analog circuit components.

The layouts introduce RC parasitic capacitance by signal paths and the way of transistor layout. The different ways of laying out the SCL inverter shows important effect on the performance and signal delay. The post-simulation shows that, the V_{swing} and switching noise are affected by the layout technique; also the total area of the circuit can be reduced significantly. The outputs of four different layouts of SCL show the effect of parasitics on signal delay and output resistance. The introduced parasitics by layouts are increased by increasing of inputs signal frequency. All post-simulation was carried out by using HSPICE, where the layout is done using Virtuoso - Cadence and the extraction done by using Mentor Graphic - Caliber Interactive tool on MIMOS 0.35u PDK.

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