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# Modeling, Simulation and Group Control of Distributed Static Series Compensators

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**Abstract:** This study investigates the new concept of Distributed Static Series Compensator (DSSC); a small, light weight cylinder that clamps directly onto the transmission line conductor and has the ability to alter the impedance of the power lines in order to increase power transfer capability and maximize economic value of the transmission system. A graphic-based simulation model of the DSSC is presented in PSCAD/EMTDC which takes into account the practical design considerations of such a device and can be considered as a starting point for extensive simulation studies. The performance and accuracy of the model is validated by simulation and comprehensive results are presented. Also a harmonic analysis of the electromagnetic model is carried out in order to investigate the amount of harmonic injection of each model and based on the results, different control strategies are applied to a group of DSSCs distributed along a transmission line. The effect of each control strategy on active power flow, THD injection and group response time is compared by simulations carried out in PSCAD/EMTDC and the most suitable control scheme for operating a group of DSSCs distributed along a typical 138 kV transmission line is presented both for capacitive and inductive compensating modes.

**Key words:** Control strategy, DSSC, PSCAD/EMTDC, active power flow, simulation model

## INTRODUCTION

In recent years many transmission lines around the world have been experiencing an increase in power transfer due to an increasing demand for electricity. While electric power demand increases considerably, additional power line constructions are often inhibited by environmental, economical and deregulation restrictions. As a result, power flow control in electric power networks is becoming one of the crucial factors of electric power system development. Therefore it is important to fully utilize the existing transmission system infrastructure by increasing the transmission capacity while having reliable control of power flow.

The concept of Flexible AC Transmission Systems (FACTS) was proposed to enhance dynamic control in power systems and to improve system utilization[1]. FACTS devices are based on the application of power electronics and high-power high-voltage converters, which can be inserted in series or shunt, or a combination of the two, to achieve many control functions such as voltage regulation, system damping and power flow control. But while FACTS devices have been proven technically and have been available over a decade, market adoption of the technology has been poor. This seems to be largely due to high cost and reliability/availability levels that may not have met utility expectations[2].

Recently a new concept from the family of distributed FACTS (D-FACTS) has been introduced as a way to remove these barriers. The concept of Distributed Static Series Compensator (DSSC) that uses a low-power single-phase inverter that attaches to the transmission conductor and dynamically controls the impedance of the transmission line, allowing control of active power flow on the line[3,4]. The DSSC concept overcomes some of the most serious limitations of FACTS devices and points the way to a new approach for achieving power flow control. A massively distributed deployment of DSSC modules on existing transmission lines would allow system operators to specify and achieve desired levels of loading on individual lines and would substantially improve the utilization of the existing power grid [5]. But in order to benefit from DSSCs an appropriate control is crucial, especially if the number of DSSCs in a grid increase or the distances between them decrease.

In this study a graphic-based simulation model of the DSSC is presented in PSCAD/EMTDC and using this model a harmonic analysis is carried out to define

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the amount of harmonic distortion injected by each DSSC. Also the effects of different control strategies applied to a group of DSSCs distributed along a transmission line are discussed and based on the results, the best control scheme for operating a group of DSSCs is presented.

## MATERIALS AND METHODS

**DSSC concept:** The concept of DSSC was introduced to illustrate the feasibility of a distributed FACTS or D-FACTS approach[6] which is a similar approach to the implementation of high power FACTS devices, but can provide higher performance and lower cost method in order to enhance system reliability and controllability.

A DSSC module as shown in Fig. 1, consists of a small rated (~10 kVA) single phase inverter and a Single Turn Transformer (STT), along with associated controls, power supply circuits and built-in communications capability[6]. The STT is a key component of the DSSC. It uses the transmission conductor as a secondary winding and is designed with a high turns ratio which reduces the current handled by the inverter and allows the use of commercial IGBTs to realize low cost. The transformer core consists of two parts that can be physically clamped around a transmission line, forming a complete magnetic circuit only after the module is clamped around the conductor[4]. Also, each module has a control circuit together with a communication system in order to have a coordinated operation when operated as a group. The weight and size of each DSSC module is low enough to allow the unit to be suspended mechanically from the power line and since it does not require supporting phase-ground insulation, the module can be applied at any line voltage ranging from 13-500 kV.

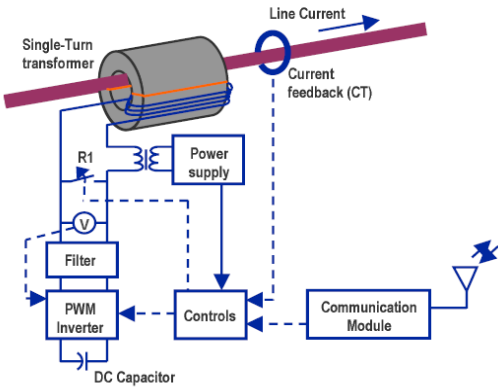


Fig. 1: Circuit schematic of a DSSC module

The operation of the DSSC can be summarized as follows: As the module starts up, the inverter voltage is in phase with the line current and real power is extracted from the line to charge the DC bus capacitor. After charging the capacitor to a predetermined voltage, the unit is controlled so that it injects a quadrature voltage or reactive impedance in series with the line, resulting in an increase or decrease of transmitted power along the transmission line[4]. When there is no longer a need for compensation, the unit is bypassed and turned off, meaning that the DSSC must have the ability to be turned on and off as many times as needed during operation. Therefore by deploying a large number of DSSC modules on a transmission line - in order to gain an adequate reactive impedance injection - the overall system benefit can only be achieved by coordinated control. This coordination can be done using an isolated communication link such as a radio receiver incorporated in each module or through the use of other commercially available communication systems such as power line communication[7].

The DSSC is connected in series with the transmission line and has the ability of injecting a synchronous fundamental voltage that is orthogonal to the line current directly into the transmission conductor, therefore the transmitted power with a DSSC connected to the line becomes a parametric function of the injected voltage ($V_q$) and can be expressed as follows[4]:

$$p_{12} = \frac{V_1 V_2}{X_L}\sin\delta - \frac{V_1 V_q}{X_L}\cos\left(\frac{\delta}{2}\right)\left[\frac{\sin\left(\frac{\delta}{2}\right)}{\sqrt{\left(\frac{V_1+V_2}{2V_2}\right)^2 - \frac{V_1}{V_2}\cos^2\left(\frac{\delta}{2}\right)}}\right] \quad (1)$$

Where:

$V_1$ and $V_2$ = The bus voltage magnitudes
$\delta$ = The voltage phase difference
$X_L$ = The impedance of the line, assumed to be purely inductive

The DSSC, can increase the transmittable power and also decrease it, simply by reversing the polarity of the injected AC voltage. Figure 2 shows, for equal bus voltage magnitudes, the variation of the transmitted power verses phase angle with different quadrature voltage injections[8].

**Simulation model:** In order to investigate the effects of DSSC on the system, an appropriate model is needed,

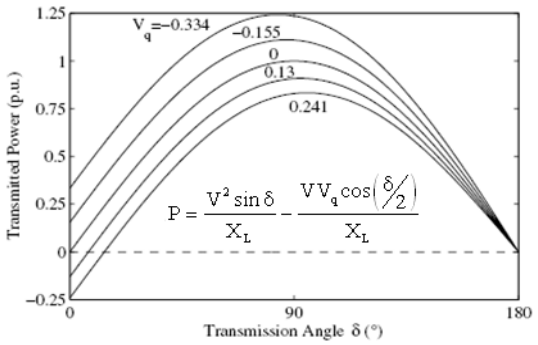


Fig. 2: Variation of transmitted power by quadrature voltage injection

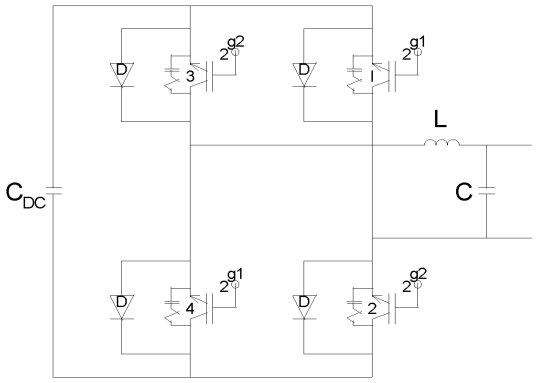


Fig. 3: Inverter of a DSSC

therefore a graphic-based PSCAD/EMTDC simulation model for the DSSC is presented here which can be suitable for electromagnetic transient studies and further operational analysis of this device.

**Inverter model:** The single phase inverter of a DSSC consists of four IGBT devices in a full bridge configuration along with an output LC filter and a DC bus capacitance as shown in Fig. 3.

The switching strategy is based on a sinusoidal pulse width modulation (SPWM) technique which offers simplicity and good response. Further more high switching frequencies can be used in this method to improve the efficiency of the converter, without incurring significant switching losses. In SPWM switching a sinusoidal waveform is compared to a triangular waveform and gate signals are generated to shape the waveform at the output of the inverter. The main parameters of the SPWM scheme are the amplitude modulation ratio ($m_a$) and the frequency modulation ratio ($m_f$) which are defined as the ratio of the peak voltage of the controlled sinusoidal waveform with that of the triangular waveform and the frequency ratio of the triangular waveform with that of the sinusoidal waveform respectively.

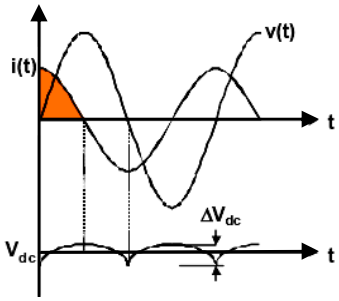


Fig. 4: Fundamental component of output voltage, current and DC capacitor voltage ripple

For the SPWM switching strategy mentioned, the amplitude modulation ratio is kept fixed at 1, in order to obtain the highest fundamental voltage component at the controller output[9]. Also the switching frequency of the triangular waveform is set to 12 kHz, in order to reduce the harmonics of the output voltage.

The output voltage of the inverter operating at high frequency is assumed to be sinusoidal with a small harmonic content. But the design of the DC bus capacitor takes into consideration only the fundamental components of the converter voltage and current. Figure 4 shows the output voltage and current of the inverter and also the voltage ripple of the DC capacitor used for reactive voltage injection in the DSSC.

The maximum ripple voltage occurs during every 1/4 period of the fundamental frequency, therefore, the area Q under the curve shown in Fig. 4 is as follows[10]:

$$Q = \int_0^{\frac{x}{2}} \sqrt{2} \times I_{rms} \times \cos(2\pi \times f \times t) dt \quad (2)$$

Where:
$I_{rms}$ = The rms current of the inverter
f = The fundamental frequency

The general equation for the DC bus capacitance where $\Delta V_{dc}$ is the maximum allowable capacitor ripple voltage is given as:

$$C_{dc} = \frac{Q}{\Delta V_{dc}} \quad (3)$$

Finally by combining (2) and (3), the final equation for the DC capacitor can be expressed as:

$$C_{dc} = \frac{I_{rms}}{\sqrt{2} \times \pi \times f \times \Delta V_{dc}} \quad (4)$$

The required DC capacitance of the presented model is determined to be around 2.5 mF for each

DSSC module, taking into account an rms current of 10 A for the inverter side and allowing a 15 V voltage ripple for the DC bus capacitor.

Since the injected voltage of a full bridge inverter contains a considerable amount of noise, therefore a low-pass LC filter is used to remove most of the switching ripple voltage and reduce the inverter output harmonics. The majority of the harmonics for a bipolar full bridge inverter are located at the switching frequency, so as far as the corner frequency selection is concerned, it is chosen such that the high frequency content is filtered. Given that the switching frequency is 12 kHz, the corner frequency should be about 10-20 times lower to be able to extract the fundamental frequency[11]. On the other hand, the fundamental frequency is not to be attenuated, so the corner frequency must be about 5 times higher than the fundamental frequency. Given these constraints, the value of the corner frequency is chosen to be around 375 Hz for the LC filter model resulting in a value of 1.8 mH for the inductance and 100 μF for the capacitance.

**Single turn transformer model:** The STT is modeled by a coupling transformer in PSCAD/EMTDC with parameters set close to that of a coaxial transformer with a small air gap in the cores magnetic path and a 1:75 ratio in order to decrease the current flowing through the inverter by a ratio of 75. This implies that under a normal line current of say 750 A for example, the inverter would only need to handle 10 A and under fault currents of 30,000 A the inverter current would only be 400 A, which is well within the capability of IGBT devices.

**Control system:** The primary function of the DSSC is to control the power flow in a transmission line. This objective can be achieved either by direct control in which both the angular position and the magnitude of the output voltage are controlled, or by indirect control in which only the angular position of the output voltage is controlled and the magnitude remains proportional to the DC terminal voltage[1]. Directly controlled inverters are more difficult and costly to implement compared to indirectly controlled inverters and their function is usually associated with some penalty in terms of increased losses, greater circuit complexity and increased harmonic content in the output. Therefore the control structure used for the DSSC model presented is based on indirect control.

The purpose of the controller is to retain the charge on the DC capacitor and to inject a voltage that is in quadrature with the line current. The DC capacitor voltage control is achieved by a small phase displacement, e, beyond the required 90° between the injected voltage and the line current. A Phase-Locked Loop (PLL) provides the basic synchronization signal, θ, which is the phase angle of the line current and the error signal obtained by comparing Vdc with Vref is passed through a PI controller which generates the required phase angle displacement or e. Also in order to reduce the voltage ripple caused by sudden phase shift, an additional control circuit is used which applies an increasing 0°~90° phase shift in less than 20ms, to prevent undesired voltage ripple and insure the stability of the system.

**Final DSSC model:** Figure 5 shows the complete circuit of the DSSC modeled in PSCAD/EMTDC,

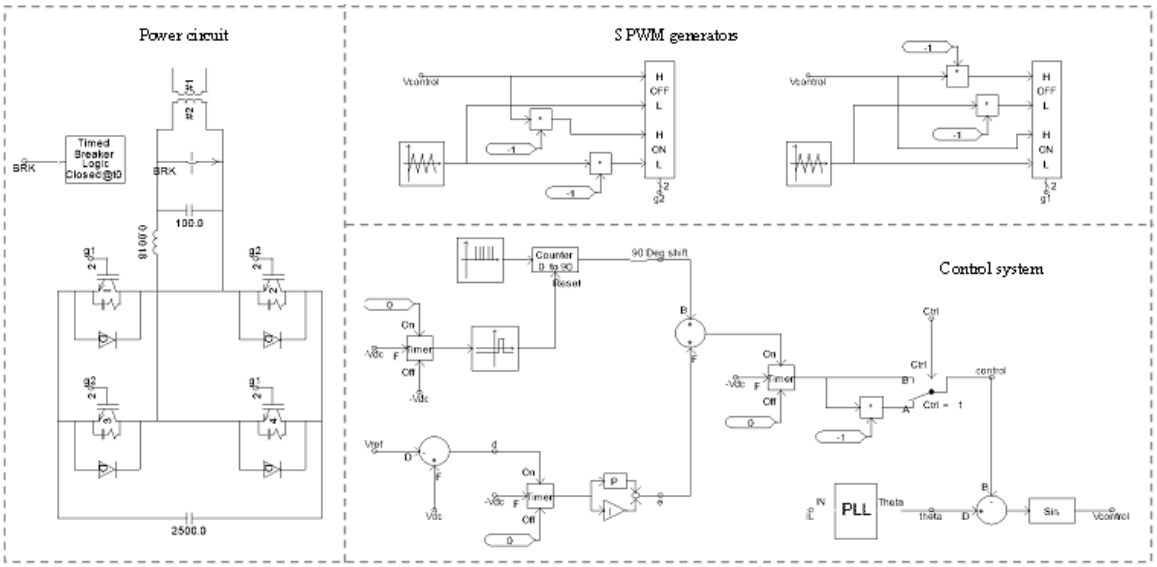


Fig. 5: Circuit model for DSSC in PSCAD/EMTDC

Table 1: Definitions of user defined DSSC model

| Parameter | Definition |
|---|---|
| V1 and V2 | Connections to the line |
| Vref | DC bus voltage reference |
| Ctrl | Capacitive (-1) or inductive (1) compensation |
| Ton | DSSC operation start time |
| Toff | DSSC operation end time |
| Vq | Injected quadrature voltage measurement |
| Vc | DC bus voltage measurement |
| IL | Line current measurement |

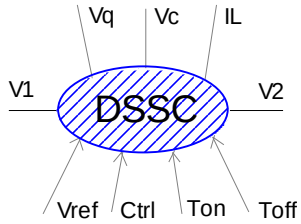


Fig. 6: User defined DSSC simulation model

including the DSSC power circuit, the sinusoidal PWM generators and the control system. A user defined DSSC model is also shown in Fig. 6, which allows the user to define all the essential control parameters of the module and can be considered as a starting point for extensive simulation studies on DSSCs. The definition of the parameters are shown in Table 1.

## RESULTS

**Simulation results:** The performance and accuracy of the presented model is validated with simulations carried out in PSCAD/EMTDC using the test system shown in Fig. 7 which consists of one DSSC model placed on each phase of a typical 138 kV transmission line with the parameters of the transmission line shown in Table 2[2].

The scenario considered in this simulation is that each DSSC starts to operate at t = 20 ms by charging its DC capacitor until the DC link voltage of the inverter reaches 1.5 kV. Then it operates to supply a leading or lagging voltage injection of 14 V which is almost orthogonal to the line current and equals to an injection of almost 10 kVAr, considering line currents of 750 A. The DSSCs are also switched off at the time of t = 2s. Figure 8-12 show the results of dynamic performance analysis of each DSSC for this simulation.

Figure 9 shows the DC bus voltage variation as the capacitor voltage is charged to 1.5 kV in less than 600 ms and the voltage is maintained at around 1.5 kV until the model is switched off, resulting in a discharge of the capacitor voltage. Figure 9 shows the voltage ripple of the DC link which is calculated to be less than %1 of the total DC bus voltage of 1.5 kV.

Table 2: Transmission line parameters

| Operating line voltage | Operating current | Impedance per kilometer | Line length used for simulation |
|---|---|---|---|
| 138 kV | 750 A | 0.104+j0.49 | 10 km |

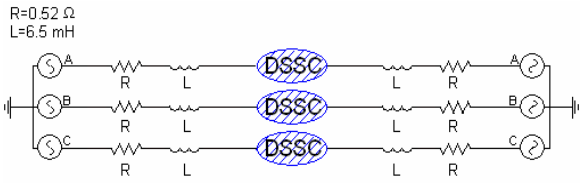


Fig. 7: Test system

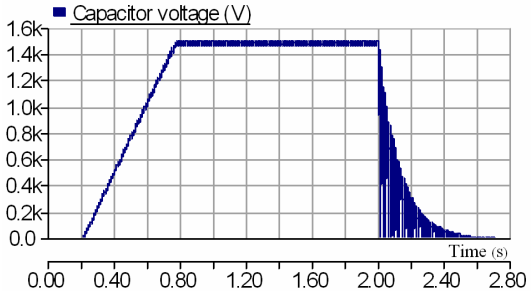


Fig. 8: DC bus voltage variation of each DSSC

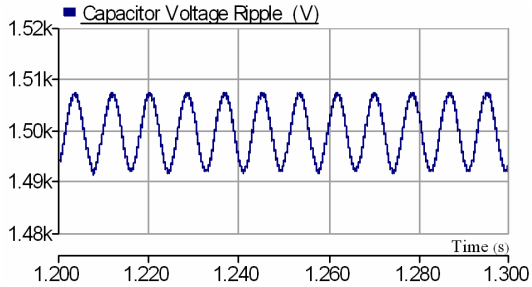


Fig. 9: DC bus voltage ripple of each DSSC

As the module starts up the inverter voltage is controlled in a way that it is in phase with the line current as shown in Fig. 10a, hence real power is extracted from the line to charge the DC bus capacitor to a predetermined voltage of 1.5 kV, from this point on the correction angle, e and the ±90° phase shift (inductive or capacitive) are applied as shown in Fig. 10b and c to accomplish reactive line compensation and also maintain the DC bus voltage.

Figure 11 and 12 show the effectiveness of the additional control circuit in applying an increasing 0°~90° phase shift in order to reduce the output voltage ripple and ensure the stability of the system.

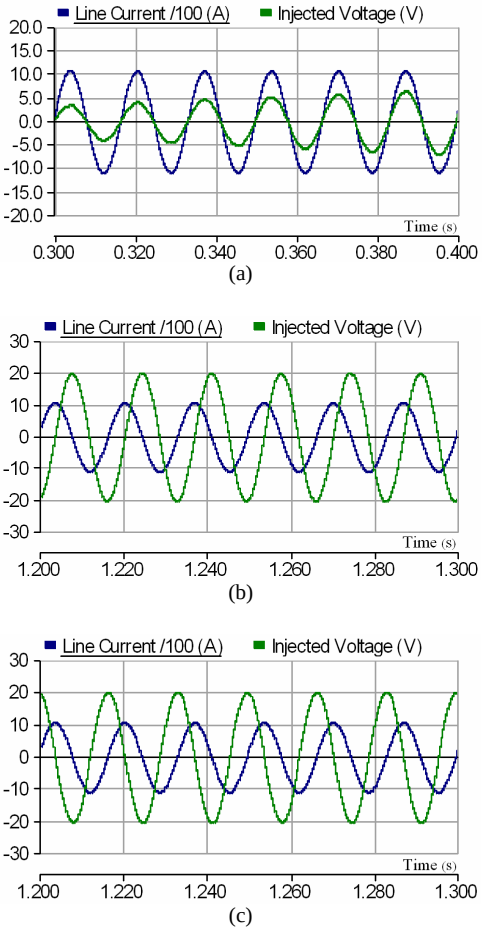


Fig. 10: DSSC voltage injection modes (a): In-phase; (b): Leading; (c): Lagging

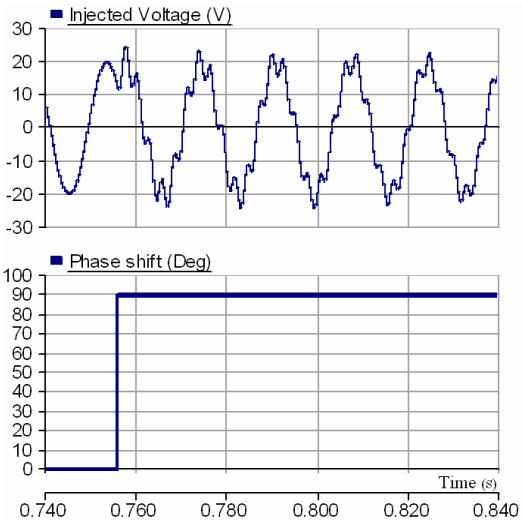


Fig. 11: Sudden phase shift effect on output voltage

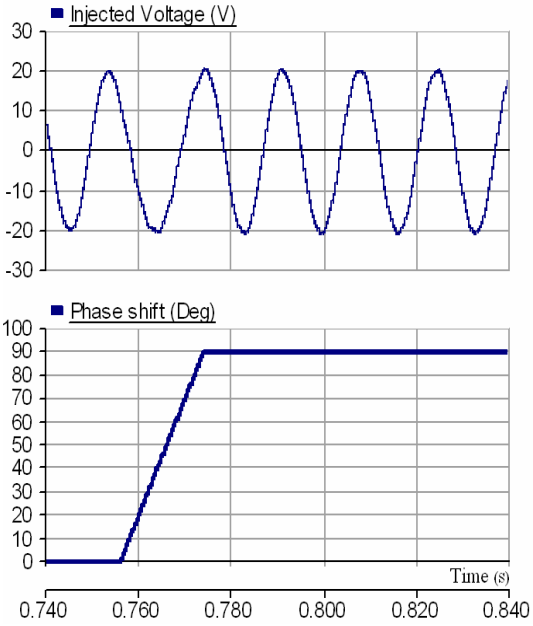


Fig. 12: Increasing phase shift effect on output voltage

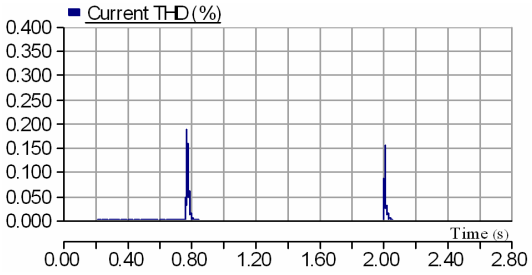


Fig. 13: THD injected to the line current by one DSSC

In order to study the effect of different control strategies on the quality of power being transmitted, a harmonic analysis was also carried out using the same test system of Fig. 7. The simulation results of THD injected to the line current are shown in Fig. 13.

Figure 13 shows the Total Harmonic Distortion (THD) injected to the line current by one DSSC module. It can be noted that the most THD injection occurs at the transition period in which the capacitor is fully charged and the voltage phase is being shifted in order to be in quadrature with the line current. There is also some harmonic injection at the time the module is switched off. Figure 14 shows the amount of THD injected to the line current by one DSSC on each phase in the time of transition and Fig. 15 shows the results of THD injection at transition time for a simulation with two DSSC modules distributed evenly along each phase of the line and operated at the same time.

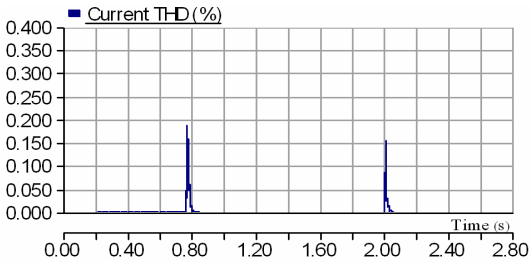


Fig. 14: THD injected in transition period by one DSSC

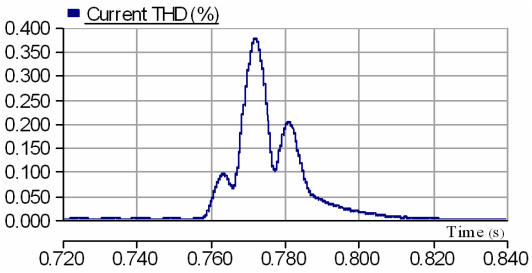


Fig. 15: THD injected in transition period by two DSSCs

The results indicate that the THD injected to the line current increases as the number of DSSC devices on each phase increase, which implies that for an adequate compensation with many DSSC devices distributed along a transmission line, a particular control algorithm is needed in order to avoid injection of harmonic distortions.

**Coordinate control of DSSCs:** A controlled transmission line implemented with multiple DSSC modules can be used to increase the capacity of an existing AC transmission system and also control the flow of power. But coordination is needed in order to achieve the fastest response time as a group while minimizing the amount of distortion injected. In this section, different control strategies are discussed for controlling a group of DSSCs distributed along a transmission line while taking into account the effect of the DSSC devices on the rest of the power system. The system used to investigate the impact of different control strategies consists of 9 user defined DSSC devices placed equally apart from each other along each phase of a typical 138 kV transmission line as shown in Fig. 16. Each user defined DSSC module has the ability to be switched on and off as desired and the transmission line is modeled by distributed parameters of a real transmission line mentioned in Table 2. The effect of each control strategy is presented in a different case and evaluated using PSCAD/EMTDC software package.

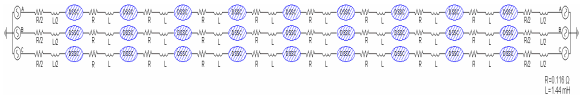

Fig. 16: System used to investigate the impact of different control strategies

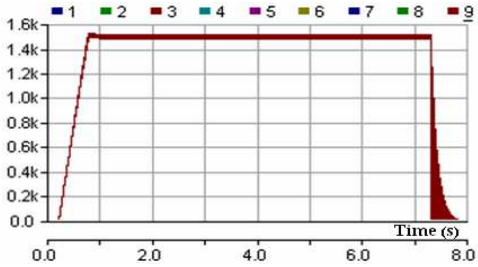


Fig. 17: DC bus voltage variation of DSSCs on each phase

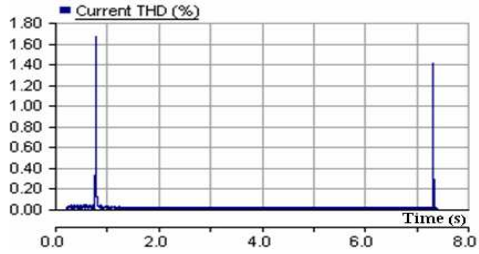


Fig. 18: THD injected by DSSCs to the line current

**Case 1:** This case represents the most simple control strategy in which all the DSSCs distributed along the transmission line are switched on at the same time of t = 0.2s and after being charged, start to compensate the line all at the same time. The DSSCs are also switched off as a group at the time of t = 7.3s. Figure 17-20 show the simulation results of this control strategy applied for two different capacitive and inductive compensation of the line.

The results of THD injection shown in Fig. 18 show that because in this control strategy all the DSSCs are switched on and charged at the same time, the maximum THD of the line current for each phase (which is estimated to be 1.7%), equals to the sum of maximum THD injections of all the DSSCs distributed in each phase of the line. Also from Fig. 19 it can be shown that in the capacitive compensation mode- in which the aim is to increase the active power being transmitted by compensating the line reactance- the transmitted power decreases by 2.48 MW as the DC bus capacitor of each DSSC module is being charged. This is because in this time period, each DSSC acts as an active impedance to the line and also extracts active power from the line in order to increase the charge on its DC bus capacitor,

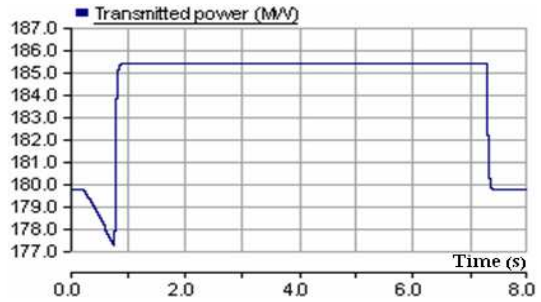


Fig. 19: Active power in capacitive compensation mode


Fig. 20: Active power in inductive compensation mode

hence the active power being transmitted is decreased for a short time. But after the capacitors are charged, the DSSCs begin to compensate the line reactance at t = 0.8s and the power is instantly increased by 8.13 MW which results in a 5.65 MW increase of power with respect to the power being transmitted before compensation. In the inductive compensation mode shown in Fig. 20, which the aim is to decrease the flow of power along the line, this control scheme has a fast and effective influence as it gradually reduces the active power flow by 2.48 MW while the capacitors are being charged and at t = 0.8s it instantly reduces the transmitted power by another 3.44 MW as a result of quadrature voltage injection and inductive compensation.

Case 2: In this case only one DSSC in each phase is switched on at t = 0.2s and the other DSSCs in each phase of the line are only switched on when the previous DSSC has been fully charged and started to compensate the line. The DSSCs in each phase are also turned off at t = 7.3s with a 40ms time delay from each other in order to prevent THD injection overlap. The simulation results of this control strategy are shown in Fig. 21-24. Results illustrate that the response time which is defined here as the time from the first DSSC being switched on until the last DSSC of the group being fully charged, is very long compared to the previous control strategy.

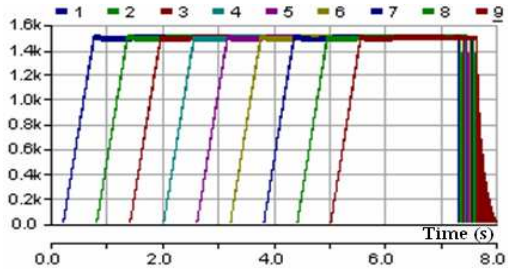


Fig. 21: DC bus voltage variation of DSSCs on each phase

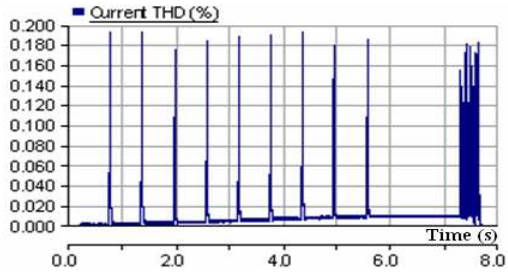


Fig. 22: THD injected by DSSCs to the line current


Fig. 23: Active power in capacitive compensation mode


Fig. 24: Active power in inductive compensation mode

Also because the DSSCs are switched and charged at different time intervals, the maximum THD injection as shown in Fig. 22 is minimized to a level of only %0.19 which is the same as the effect of one DSSC on each phase.

It can be shown from Fig. 23 that the first DSSCs to be switched on in each phase reduce the power by 0.27 MW while being charged and increase it by about 0.58 MW when compensating in capacitive mode. Therefore, by applying this control strategy for capacitive compensation, the initial reduction in power flow is limited to only 0.27 MW.

**Case 3:** The results obtained from the two previous strategies indicate that in order to minimize the injection of harmonic distortion of DSSCs as a group, they should be controlled such that no two DSSCs in one phase are switched on at the same time and a time delay of about 40 ms is adequate in order to prevent an overlap of maximum THD injection areas of the DSSC modules. It can also be noted that in the capacitive compensation mode neither of the two strategies discussed can simultaneously provide a fast response and minimize power flow tolerance. Therefore a third strategy is presented based on the results obtained from previous cases that when one DSSC on each phase is being charged, the power flow along the transmission line is decreased by 0.27 MW as a result of active power being extracted from the line in order to charge the DC bus capacitor, but on the other hand when the DSSC is fully charged and is operating in a capacitive compensation mode, its influence on increasing the power flow is about 0.58 MW. Hence the reduction effect of two DSSCs being charged can be cancelled out by one DSSC capacitively compensating the line, therefore for this control strategy, the number of DSSCs to be switched on at each time interval for each phase can be calculated by Eq. 5, simply by doubling the number of DSSCs already active and compensating the line. Where $M_n$ is the number of DSSCs switched on at each time interval (n). Also for each set of DSSCs switched on at the same time there is a 40ms time delay in order to eliminate the THD injection overlap and ensure a lower harmonic injection:

$$M_n = \begin{cases} 1 & n = 1 \\ 2\sum_{x=1}^{n-1} M_x & n = 2,3,4... \end{cases} \quad (5)$$

The simulation results of this control strategy applied for capacitive and inductive compensation of the line are shown in Fig. 25-28 in which the number of DSSCs switched on in each phase for 3 time intervals are calculated and shown in Table 3. Also the DSSCs are switched off with a 40ms time delay from each other at t = 7.3s.

Table 3: DSSCs switch on time for 3 time Intervals

| Time interval (n) | No. of DSSCs switched on (Mn) | Switch on time |
|---|---|---|
| 1 | 1 | 0.20 sec |
| 2 | 2 | 0.80 sec |
| | | 0.84 sec |
| 3 | 6 | 1.44 sec |
| | | 1.48 sec |
| | | 1.52 sec |
| | | 1.56 sec |
| | | 1.60 sec |
| | | 1.64 sec |

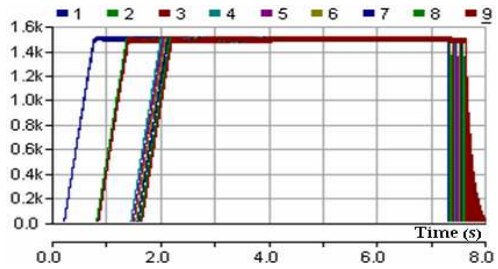


Fig. 25: DC bus voltage variation of DSSCs on each phase

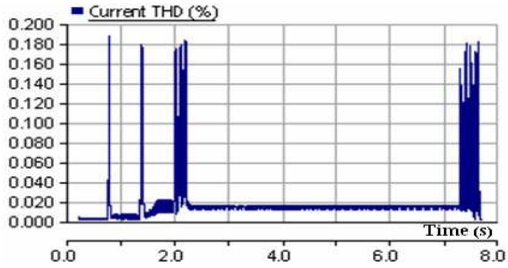


Fig. 26: THD injected by DSSCs to the line current


Fig. 27: Active power in capacitive compensation mode


Fig. 28: Active power in inductive compensation mode

Table 4: Results of Different Control Strategies

| Control strategies | Strategy 1 | Strategy 2 | Strategy 3 |
|---|---|---|---|
| MAX THD Injection | 1.7% | 0.19% | 0.19% |
| Group response time | 0.6 sec | 5.4 sec | 2.04 sec |
| Initial power flow reduction | 2.48 MW | 0.27 MW | 0.27 MW |
| **Total change in power flow** | | | |
| Capacitive | +5.65 MW | +5.65 MW | +5.65 MW |
| Inductive | -5.92 MW | -5.92 MW | -5.92 MW |

The results indicate that with this control strategy applied, the amount of THD injection to the line current for both the capacitive and inductive compensation is kept well below 0.19%. Also in the capacitive compensation mode the power flow reduction at the beginning is limited to 0.27 MW which was also obtained by the second control strategy, but the advantage of this algorithm is that despite reducing the power flow tolerance it has a faster response time compared to the second control strategy.

## DISCUSSION

In order to compare the effect of each control strategy on power flow, response time and power quality, results obtained from each case are shown in Table 4. It can be shown from Table 4 that all 3 strategies have the same effect on the total change in power flow but strategy 2 and 3 have the least reduction in initial power flow and among these two, strategy 3 has the fastest group response time. Therefore if the aim of controlling a group of DSSCs operating in capacitive mode, is to minimize power flow tolerance and THD injection with an acceptable response time, strategy 3 has an advantage over the other two strategies discussed. As for the inductive compensation mode, (in which the aim is to decrease the flow of power) strategy 1 achieves the fastest response time but injects the most harmonic distortion to the line. However, this harmonic injection can be decreased if the DSSCs are switched on with a 40ms time delay from each other. Although this time delay will have an effect on the response time, but strategy 1 would still possess the fastest response time compared to the other two strategies. Therefore, in the inductive mode, strategy 1 (with some changes) is the best control strategy applied to a group of DSSCs.

## CONCLUSION

In this study a detailed model of the DSSC is used to study and simulate the effect of different control strategies applied to a group of DSSCs distributed along a transmission line. Simulation results indicate that the transmitted power along the line decreases as the DC bus capacitor of each DSSC module is being charged and the harmonic distortion introduced by each DSSC device is maximum at a time when the DC bus capacitor is fully charged and the device is starting to inject a voltage that is almost in quadrature with the line current. Therefore, one way of reducing harmonic injection of DSSC devices as a group is to allow a 40ms time delay between each switch on, in order to eliminate the overlapping of maximum harmonic injection zones. Also, based on the simulation results of 3 different scenarios, it is concluded that the best control strategy for controlling a group of DSSCs can be obtained by applying strategy 3 for capacitive compensation mode and strategy 1 (with minor adjustments) for inductive compensation mode of operation.

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