Field Programmable Gate Arrays based Design, Implementation and Delay Study of Braun's Multipliers

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Abstract:Problem statement: Parallel array multipliers are required to achieve high execution speed for Digital Signal Processing (DSP) applications. **Approach:** The purpose of this article is to investigate Field Programmable Gate Arrays (FPGAs) implementation of standard Braun's multipliers on Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5 FPGAs using Very high speed integrated circuit Hardware Description Language (VHDL). The delay study was analyzed using Analysis Of Variance (ANOVA) method using the software Statistical Package for Social Science (SPSS) with a 0.05 confidence level was used to compare the FPGA devices. **Results:** The FPGA resource utilization by Virtex-5 is the lowest in value for 4×4, 6×6, 8×8 and 12×12-bit Braun's multipliers as compared to Spartan-3AN, Virtex-2 and Virtex-4 FPGAs. The average connection delays in Virtex-2 shows consistency and gradual increase in value as the size of multiplier increased. Virtex-2 FPGA demonstrates lower average connection delays as compared to Spartan-3AN, Virtex-4 and Virtex-5 FPGAs. For the maximum pin delay same observations are obtained for Virtex-2 FPGA. The anomalies in maximum pin delay and average connection delay are observed in Virtex-5, Virtex-4 and Spartan-3AN FPGAs. FPGA devices also demonstrate that as the size of multipliers increases their mean latency value is also increases. **Conclusion:** The FPGA resource utilization by Virtex-5 is the lowest in value for 4×4, 6×6, 8×8 and 12×12-bit Braun's multipliers as compared to Spartan-3AN, Virtex-2 and Virtex-4 FPGAs. Even value obtained for Virtex-5 FPGA for 4×4 bit standard Braun's multiplier for number of occupied slices and look up tables are lower in value than reported in literature.

Key words: Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), Spartan-3AN, Digital Signal Processing (DSP),General Purpose Signal Processor (GPSP)

INTRODUCTION

Computational complexities of algorithms require fast and efficient parallel multipliers for Digital Signal Processing (DSP) applications. Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT) and Inverse Discrete Cosine Transform (IDCT) involve multiplication intensive algorithms commonly implemented by DSP hardware. Implementation of DSP applications require the algorithms should be verified and optimized before realization. Multiplication has always been hardware- time-and power-consuming computation in airthematic operations. In many cases implementation of DSP algorithm demands using Application Specific Integrated Circuits (ASICs). This is especially required for image processing applications. Since development costs for ASICs are high, algorithms should be verified and optimized before implementation. Field Programmable Gate Arrays (FPGAs)can provide such optimization and implementation of algorithms in real time frame.

A number of research efforts have been reported for making low power multipliers (Al Mijalli, 2011a; 2011b; Rais, 2009a; 2009b; Rais, 2010a; 2010b; Rais et al., 2010; Rais and Al Mijalli, 2011a; 2011b; 2011c).

The objective of this study is to present study of standard Braun's multipliers (Yeo and Roy, 2005) using Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5 FPGA devices. And also to present the statistical evaluation effect of the Braun's multipliers delays in FPGA devices using Analysis Of Variance (ANOVA) and post hoc

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Tukey's test using the Statistical Package for Social Science (SPSS).

MATERIALS AND METHODS

Architecture platform: FPGAs especially find applications in algorithms that can make use of the massive parallelism offered by their architecture. Significant speedup in computation time can be achieved by assigning computation intensive tasks to hardware and by exploiting the parallelism in algorithms. FPGAs enable a high degree of parallelism and can achieve orders of magnitude speedup over General Purpose Processors (GPPs). This is a result of increasing embedded resources available on FPGA. The inherent parallelism of the logic resources on an FPGA allows for considerable computational throughput even at a low MHz clock rates. The flexibility of the FPGA allows for even higher performance by trading off precision and range in the number format for an increased number of parallel arithmetic units. This has driven a new type of processing called reconfigurable computing, where time intensive tasks are offloaded from software to FPGAs.

Spartan-3 FPGAs: The Spartan-3 FPGA (Xilinx, 2009) is specifically designed to meet the needs of high volume, low unit cost electronic systems. The family consists of eight member offering densities ranging from 50,000 to five million system gates. The Spartan-3 FPGA consists of five fundamental programmable functional elements: CLBs, IOBs, Block RAMs, dedicated multipliers (18×18) and Digital Clock Managers (DCMs). Spartan-3 family includes Spartan-3L, Spartan-3E, Spartan-3A, Spartan-3A DSP, Spartan-3AN and the extended Spartan-3A FPGAs. Particularly, the Spartan-3AN is used as a target technology in this study.

Virtex-2 FPGAs: The Virtex-2 FPGA family Xilinx, 2007, is a platform developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video and DSP applications, including PCI, LVDS and Double-Data-Rate (DDR) interfaces. The leading-edge 0.15-0.12μm CMOS 8-layer metal process and the Virtex-2 architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates,

the Virtex-2 family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. The Virtex-2 family comprises 11 members, ranging from 40K-8M system gates. The Virtex-2 architecture is optimized for high-density and high-performance logic designs.

The Virtex-2 FPGA family consists of four major elements such as Configurable Logic Blocks (CLBs), Block Select RAM, 18×18-bit dedicated multipliers and Digital Clock Manager (DCM).

Virtex-4 FPGAs: Viretx-4 FPGAs Xilinx, 2007 consists of three platform families i.e., LX, SX and FX. Virtex-4 devices consumes approximately 50% the power of respective Virtex-2 Pro devices due to static and dynamic power reduction enabled by triple-oxide technology and reduced core voltage and capacitance respectively. The Virtex-4 FPGA family comprises of CLBs, Block RAMs, Xtreme DSP Slices and DCMs.

Virtex-5 FPGAs: The Virtex-5 FPGA devices Xilinx, 2007 are a programmable alternative to custom ASIC technology. Virtex-5 family provides power-optimized high speed serial transceiver blocks for enhanced serial connectivity, tri-mode Ethernet MACs and high-performance PPC 440 microprocessor embedded blocks. Virtex-5 devices also use triple-oxide technology for reducing the static power consumption. Their 1.0V core voltage and 65nm implementation process leads also to dynamic power consumption reduction as compared to Virtex-4 devices. Advanced DSP48E slices are available in Virtex-5 FPGAs that helps in accelerating computation intensive DSP and image processing algorithms.

Braun's multipliers: Braun's multiplier is an m×n bit parallel multiplier and generally known as carry save multiplier and is constructed with m× (n-1) adders and m×n and gates. The Braun's multiplier has a glitching problem which is due to the ripple carry adder in the last stage of the multiplier.

Mathematical basis of braun's multiplier: Consider a generic m by n multiplication of two unsigned n-bit numbers $Y = Y_{m-1} .... Y_0$ and $X = X_{n-1...} X_0$:

$$Y = \sum_{i=0}^{m-1} Y_i 2^i$$

$$X = \sum_{i=0}^{n-1} X_i 2^i$$

The product $P = P_{2n-1} \ldots P_1 P_0$, which results from multiplying the multiplicand Y by the multiplier X, can be written as follows:

$$P = \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} (Y_i X_j) 2^{i+j}$$

RESULTS

FPGA design and implementation and one way ANOVA statistics: The design of standard Braun's multipliers are done using VHDL and implemented in a Xilinx Spartan-3AN XC3S700AN (package: fgg484, speed grade: -5), Virtex-2 XC2V40 (package: fg256, speed grade: -6), Virtex-4 XC4VLX40 (package: ff668, speed grade: -12) and Virtex-5 XC5VLX50 (package: Ff676, speed grade: -3) FPGAs using the Xilinx ISE 9.2i design tool Xilinx, 2007. A one-way ANOVA is applied to compare the mean delay time for four devices, Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5. The delay time for these devices is calculated using four multipliers 4×4, 6×6, 8×8 and 12×12. The statistical analysis is done by using SPSS program.

DISCUSSION

Table 1 summarizes the statistics of delay in Braun's multipliers for Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5 FPGAs. The lowest mean value is obtained for 4×4 bit multiplier for Virtex-5 is 6.58 ns as compared to Virtex-2, Virtex-4 and Spartan-3AN are 7.84, 9.5 and 12.06 ns respectively. The Virtex-5 FPGA also demonstrates lowest mean values for 6×6, 8×8 and 12×12 bit Braun's multipliers.

Tables 2-5 summarize the Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5 FPGAs devices resources utilization for standard 4×4, 6×6, 8×8 and 12×12-bit Braun's multipliers. The FPGA resource utilization by Virtex-5 are the lowest in value for 4×4, 6×6, 8×8 and 12×12-bit Braun's multipliers as compared to Spartan-3AN, Virtex-2 and Virtex-4 FPGAs. Even value obtained for Virtex-5 FPGA for 4×4 bit standard Braun's multiplier for number of occupied slices and look up tables are lower in value than reported in (Anitha and Bagyaveereswaran, 2011).

Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5 FPGA devices demonstrate that as the size of multipliers increases their mean latency value is also increases.

Table1: Statistics of latency in Braun's multipliers for FPGAs

FPGA devices	Bit width	Mean (ns)	Std. deviation (ns)	Std. error of mean (ns)
Spartan-3AN	4×4	12.06	0.7162	0.3203
	6×6	13.46	0.5177	0.2315
	8×8	17.22	0.9365	0.4188
	12×12	19.84	1.2837	0.5741
Virtex-2	4×4	7.84	0.4278	0.1913
	6×6	10.36	0.9659	0.4320
	8×8	12.50	0.7906	0.3536
	12×12	16.36	0.2702	0.1208
Virtex-4	4×4	9.50	0.5788	0.2588
	6×6	12.06	0.4278	0.1913
	8×8	11.74	0.2191	0.0980
	12×12	14.38	0.7727	0.3455
Virtex-5	4×4	6.58	0.2588	0.1158
	6×6	8.14	0.2881	0.1288
	8×8	8.60	0.1581	0.0707
	12×12	12.78	0.1304	0.0583

The same finding is obtained here as reported in Al Mijalli (2011a and 2011b); Rais and Al Mijalli (2011c) that as the size of multiplier increases the mean delay time also increases.

The one-way ANOVA on Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5 FPGAs are shown in Table 6. There is a statistically significant difference at the 0.05 level in delay time for the four devices [$F_{(3, 76)}$ = 19.546, p = 0.000] compared by using ANOVA and post-hoc Tukey HSD multiple comparison tests at the 0.05 significance level. The test indicates that the mean of delay time for Virtex-5 (Mean = 9.03, Standard Deviation = 2.36) is significantly different from the other three devices; Spartan-3AN (Mean = 15.65, Standard Deviation = 3.26), Virtex-2 (Mean = 11.77, Standard Deviation = 3.26) and, Virtex-4 (Mean = 11.92, Standard Deviation = 1.84). However, there is no statistically significant difference in mean delay times of the devices between Virtex-2 and Virtex-4.

Average connection delays are much lower in Virtex-2 FPGA as compared to Spartan-3AN, Virtex-4 and Virtex-5 FPGAs. As well as there is consistency and gradual increase is seen in Virtex-2 average connection delay. For the maximum pin delay same observation is obtained for Virtex-2 FPGA that the values are gradually increasing as the size of multiplier increases. The anomalies in maximum pin delay and average connection delay are observed in Virtex-5, Virtex-4 and Spartan-3AN FPGAs.

Figure 1 shows the average value of mean delay time for Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5 FPGAs devices for 4×4, 6×6, 8×8 and 12×12 Braun's multipliers, which clearly indicate that the average value of mean delay time for Virtex-5 is much lower in value than Spartan-3AN, Virtex-4 and Virtex-2 FPGAs.

Table 2: FPGA resource utilization for standard braun's multipliers for spartan-3AN XC3S700AN (package: fgg484, speed grade:-5) (Rais and Al Mijalli, 2011c)

Bit width	Multipliers	Four input LUTs (11776)	Occupied slices (5888)	Bonded IOBs (372)	Total equivalent gate count	Average connection delay (ns)	Maximum pin delay (ns)
n = 4	Standard	32	17	16	192	1.336	3.425
n = 6	Standard	75	40	24	450	1.007	2.835
n = 8	Standard	133	69	32	798	1.325	4.187
n = 12	Standard	295	152	48	1770	1.020	4.626

Table 3: FPGA resource utilization for standard braun's multipliers for virtex-2 XC2V40 (package: fg256, speed grade: -6)

Bit width	Multipliers	Four input LUTs (512)	Occupied slices (256)	Bonded IOBs (88)	Total equivalent gate count	Average connection delay (ns)	Maximum pin delay (ns)
n = 4	Standard	32	17	16	192	0.489	1.368
n = 6	Standard	75	40	24	450	0.592	1.646
n = 8	Standard	133	69	32	798	0.713	2.116
n = 12	Standard	295	152	48	1770	0.795	2.450

Table 4: FPGA resource utilization for standard braun's multipliers for Virtex-4 XC4LX40 (package: ff668, speed grade: -12)

Bit width	Multipliers	Four input LUTs (36864)	Occupied slices (18432)	Bonded IOBs (448)	Total equivalent gate count	Average connection delay (ns)	Maximum pin delay (ns)
n = 4	Standard	32	17	16	192	1.037	2.754
n = 6	Standard	75	40	24	450	0.924	2.245
n = 8	Standard	133	70	32	798	0.923	2.333
n = 12	Standard	295	152	48	1770	0.957	3.011

Table 5: FPGA resource utilization for standard braun's multipliers for Virtex-5 XC5VLX50 (package: ff676, speed grade:-3)

Bit width	Multipliers	Four Input LUTs (28800)	Occupied slices (7200)	Bonded IOBs (440)	Total equivalent gate count	Average connection delay(ns)	Maximum pin delay (ns)
n = 4	Standard	22	11	16	154	0.887	2.103
n = 6	Standard	43	19	24	301	0.885	1.795
n = 8	Standard	81	29	32	567	0.857	1.733
n = 12	Standard	202	96	48	1414	1.074	2.834

Table 6: The results of multiple comparisons of delay time (ns) for four devices using the Tukey's HSD post-hoc test

(I) Devices	(J) Devices	Mean difference (I-J)	Std. Error	Sig	95% Confidence interval Lower bound	Upper bound
Spartan-3AN	Virtex-2	3.88000*	0.86952	0.000	1.596	6.164
	Virtex-4	3.72500*	0.86952	0.000	1.441	6.009
	Virtex-5	6.62000*	0.86952	0.000	4.336	8.904
Virtex-2	Spartan-3AN	-3.88000*	0.86952	0.000	-6.164	-1.596
	Virtex-4	-0.15500	0.86952	0.998	-2.439	2.129
	Virtex-5	2.74000*	0.86952	0.012	0.456	5.024
Virtex-4	Spartan-3AN	-3.72500*	0.86952	0.000	-6.009	-1.441
	Virtex-2	0.15500	0.86952	0.998	-2.129	2.439
	Virtex-5	2.89500*	0.86952	0.007	0.611	5.179
Virtex-5	Spartan-3AN	-6.62000*	0.86952	0.000	-8.904	-4.336
	Virtex-2	-2.74000*	0.86952	0.012	-5.024	-0.456
	Virtex-4	-2.89500*	0.86952	0.007	-5.179	-0.611

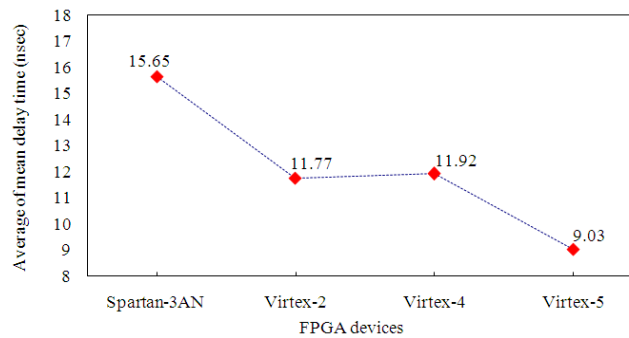*: The mean difference is significant at the 0.05 level

Fig. 1: Average of mean delay time for Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5 for the Braun's multipliers

CONCLUSION

We have presented hardware design and implementation of FPGA based parallel architecture for standard Braun's multipliers using VHDL. The design was implemented on Xilinx Spartan-3AN XC3S700AN, Virtex-2 XC2V40, Virtex-4 XC4VLX40 and Virtex-5 XC5VLX50 FPGA devices using the ISE 9.2i design tool. The FPGA resource utilization by Virtex-5 is the lowest in value for 4×4, 6×6, 8×8 and 12×12-bit Braun's multipliers as compared to Spartan-3AN, Virtex-2 and Virtex-4 FPGAs. Even value obtained for Virtex-5 FPGA for 4×4 bit standard Braun's multiplier for number of occupied slices and look up tables are lower in value than reported in literature. Average connection delays are much lower in Virtex-2 FPGA as compared to Spartan-3AN, Virtex-4 and Virtex-5 FPGAs. As well as there is consistency and gradual increase is seen in Virtex-2 average connection delay. For the maximum pin delay same observation is obtained for Virtex-2 FPGA that the values are gradually increased as the size of multiplier increases. The anomalies in maximum pin delay and average connection delay are observed in Virtex-5, Virtex-4 and Spartan-3AN FPGAs.

There is a statistically significant difference at the 0.05 level in delay time for the four devices compared by using ANOVA and post-hoc Tukey HSD multiple comparison tests at the 0.05 significance level. The test indicates that the mean of delay time for Virtex-5 and Spartan-3AN are significantly different from the other two devices; Virtex-2 and Virtex-4 FPGAs. However, there is no statistically significant difference in mean delay times of the devices between Virtex-2 and Virtex-4.

Spartan-3AN, Virtex-2, Virtex-4 and Virtex-5 FPGA devices also demonstrates that as the size of multipliers increases their mean latency value is also increases.

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