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Fault Detection and Classification in Power Electronic Circuits Using Wavelet Transform and Neural Network

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Abstract: Problem statement: The identification of faults in any analog circuit is highly required to ensure the reliability of the circuit. Early detection of faults in a circuit can greatly assist in maintenance of the system by avoiding possibly harmful damage borne out of the fault. **Approach:** A novel method for establishing a fault dictionary using Wavelet transform is presented. The Circuit Under Test (CUT) is three phase single level inverter. The transform coefficients for the fault free circuit as well as for the simulated faults of CUT are found. The Wavelet transform is applied to the output of CUT and Standard Deviation (SD) of the transform coefficients are extracted. Using the transform coefficients, fault dictionary has been formed. In order to identify the type of fault, a neural network classifier has been utilized. **Results:** The compatibility of wavelet analysis with the various classification techniques for fault diagnosis has been illustrated in this study. The results of the study demonstrate the suitability and viability of wavelet analysis in fault diagnosis of power electronic circuits. **Conclusion:** The proposed approach is found to be more reliable in accurate identification and isolation of faults using fault dictionary. Moreover, the neural classifier improves the efficiency of the system as neural networks do not require prior knowledge as they are capable of learning and evolving through a number of learning algorithms.

Key words: Fault diagnosis, wavelet transform, three phase inverter, fault dictionary, neural network classifier, Circuit Under Test (CUT), Standard Deviation (SD), Fault Detection and Isolation (FDI), Simulation-After-Test (SAT), Simulation-Before-Test (SBT)

INTRODUCTION

Nowadays, the prime focus of industries is in the field of control engineering. It concerns mainly to monitor a system, detect the occurrence of fault in the system and identify the type of fault and its location. This is mainly to done to protect the system and avert any possible damages borne out of the fault.

Fault Detection and Isolation (FDI) is an integral part of the diagnostic system to ensure the reliability and safety of the system under study. A sustained unexpected behavior of the circuit is said to be a faulty circuit. There are two kinds of failure modes in analog circuits, namely catastrophic and parametric fault. A set of parametric faults are difficult to build while catastrophic faults may be derived from its layout for analog IC.

Fault diagnosis approaches are of many types namely, fault dictionary approach, the parameter identification approach, the fault verification approach, the approximation approach, the artificial intelligence technique and so on. (Mamat *et al*., 2006; Lee and Bedrosian, 1979; Manikandan and Devarajan 2007; Prasannamoorthy *et al*., 2010). In general, the fault diagnosis approaches of analog circuit can be categorized into two namely, Simulation-Before-Test (SBT) and Simulation-After-Test (SAT). The various parameters that are required to build in the fault dictionary are being extracted from the operational circuit in the case of SAT. Assuming that the each parameter is independent of the other, fault identification is being carried out. But when the size of the circuit is increased, the processing time is also increased. Hence this method is usually avoided. While in SBT approach (Guillaume, 2001; Mckeon and Wakeling, 1989; Dubois and Prade, 1980; Gertler, 1998; Manikandan and Devarajan, 2007) the operation time is reduced as the signatures are extracted by simulating a finite set of arbitrary test conditions that are unique to each faulty condition.

As both the procedures are procedural in nature the intuitional knowledge of the functioning of the CUT is not required. The signatures can be suitably used to create a fault dictionary, which is a collection of

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measurement of a network under different potential faults. The condition for avoiding masking of any faults is that the parameters chosen for signatures must be observable for all conditions of the circuit.

Fault diagnosis is a combination of fault detection and isolation. Early detection of fault can possibly avoid the damages borne out of the fault. This can ensure safety and reliability of the circuit. The most prominent sources of fault in a power electronic circuit are the semiconductors. The faults can be either short circuit faults or open circuit faults. The latter is very rare but it may create overstress on other component leading to its failure.

The voltage source inverter is chosen as the CUT. A three phase single level IGBT VSI was modeled using MATLAB. Its each phase was analyzed using wavelet transform. The standard deviation of the transform coefficients is fed as input to the neural network classifier, designed specifically to identify the fault type.

Wavelet theory: Wavelet mean 'small wave'. Its nomenclature as a wave can be attributed to its oscillatory nature. The wavelet analysis involves analyzing a signal with short duration finite energy functions. Thus the signal under investigation is being transformed into another representation of more useful format. This signal transformation is called Wavelet Transform. Wavelet can be manipulated in two ways, translation and scaling. Mathematically, a wavelet can be denoted as:

$$\psi_{a,b}(x) = \frac{1}{\sqrt{a}}\psi\left(\frac{x-b}{a}\right),\ a < 0$$

Where:
b = Location parameter
a = Scaling parameter

Generally, wavelet transform is used as a tool to decompose functions or operators into diverse frequency components. The transform is computed generally at various locations of the signal and for various scales of the wavelet, thus filling up the transform plane. If the process is done in a smooth and continuous fashion, then the transform is called Continuous Wavelet Transform (CWT). If the scale and position are changed in discrete steps, the transform is called Discrete Wavelet Transform (DWT).

Continuous wavelet transform is defined by the inner product of the function and basis wavelet:

$$CWT_f(a,b) = \frac{1}{\sqrt{a}}\int_{-\infty}^{\infty} f(x)\psi\frac{\overline{x-b}}{a}dx$$

According to this equation for every (a,b), we have a wavelet transform coefficient, representing how much the scaled wavelet is similar to the function at location x = (b/a). The practical application of CWT is limited by the redundant and non-finite nature of the coefficients. These coefficients are obtained by the correlation of the function and the wavelet performed during the continuous translation and scaling of the wavelet. Discretization is therefore resorted to, the time scale plane being discretized into grid nodes at which the CWT is performed. The generation of fast algorithms calls for the development of discrete wavelets, which are usually part by part continuous functions.

Generalized algorithm: The fault diagnosis methodology may be divided into the following distinct steps:

- Formulation of a model of the CUT, which is a three phase single level inverter in this case
- Application of the wavelet transforms for the various fault condition as well as fault free condition
- Building a fault dictionary by extracting the standard deviation of the transform coefficients
- Identifying the fault type by using the parameters of the CUT in a neural network classifier

Circuit under test: A three phase single level IGBT Voltage Source Inverter (VSI) as shown in Fig. 1 was chosen.

The model of the circuit consists of a 400V DC and a series RLC circuit as an arbitrary load. A resistance of 1000 Ω and an inductance of 5H and a capacitance of 0.006F were assumed in the construction of the model. The necessary gating signals to the thyristor switches have been provided by the pulse generators operating at 50% duty cycle.

The open circuit and short circuit fault are simulated by the circuit model as shown in the Fig. 2. (Open circuit fault) and in the Fig. 3. (Short circuit fault).

The former fault is simulated by removing the gating pulse for the semiconductor switch. This is done by disconnecting the function generator. This model is based on the assumption of ideality of the semiconductor that may not conduct in the absence of a gate signal, thus acting as an open circuit. While the latter fault is simulated by bypassing the IGBT switch.

The output voltage waveform of phase A, phase B and phase C corresponding to open circuit fault at IGBT4, designated OF4, has been provided in Fig. 4-6 respectively.

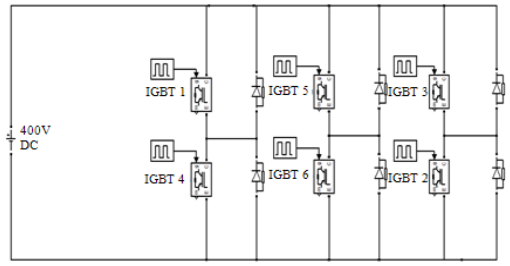

Fig. 1: Three phase single level inverter

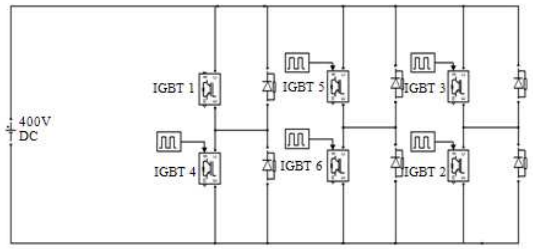

Fig. 2: Open circuit fault-IGBT1 is assumed to be open

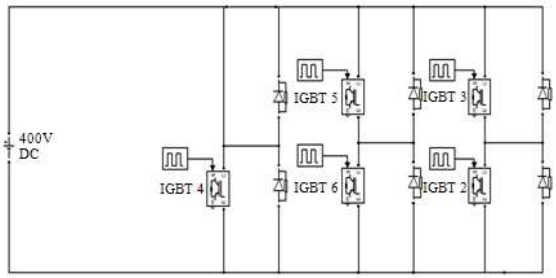

Fig. 3: Short circuit fault-IGBT1 is assumed to be short circuited

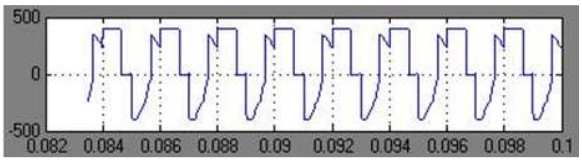

Fig. 4: Output voltage waveform for phase A for fault OF4

Signature extraction: The signatures for each fault condition as well as for the fault free condition have to be extracted to build the fault dictionary. This utilizes the statistical analysis of transform coefficients. In this study, single as well as double faults have been considered. However, this technique can be extended to higher degree of faults without any change in the methodology.

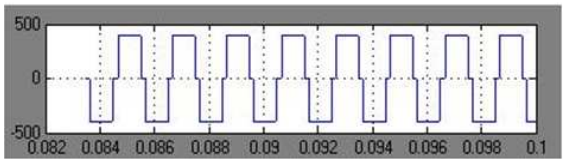

Fig. 5: Output voltage waveform for phase B for fault OF4

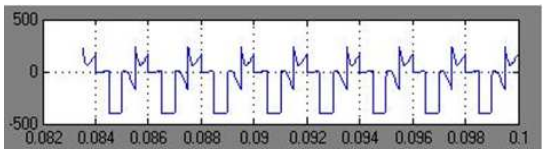

Fig. 6: Output voltage waveform for phase C for fault OF4

In a three phase single level inverter circuit consisting of 6 thrusters, there is a possibility for the occurrence of 6 open circuit and 6 short circuit single faults and 15 open circuit and 15 short circuit double faults. Owing to the aberration in the output due to the short circuit of the voltage source, the cases of short circuit double faults in which both the faults occur in switches belonging to the same arm have been dropped out. The absence of any output voltage in the fault free legs leads to the failure of any attempt to perform wavelet transform.

The output voltage of each phase is analyzed using Wavelet Toolbox in MATLAB. The choice of the mother wavelet used is primarily influenced by the occurrence of redundancies in the signatures. The wavelets which do not pose redundancy problems are further prioritized based upon the efficiency of the classifier when operated in tandem. The performance of each wavelet for individual CUTs differs thereby postulating a detailed performance analysis of the various wavelets.

After a detailed analysis, the Symlet-2 wavelet qualified as the wavelet of choice. The wavelet was employed at fifth level of detail. This is highly important because the level of detail has a marked impact on the efficiency of the classifier. Higher the level of detail chosen for extraction, greater is the efficiency. Thus the choice of level of detail involves a trade-off between efficiency and simplicity.

The transformation is being followed by statistical analysis. The Standard Deviation (SD) was chosen as the statistical parameter. This is due to the fact that SD spans a finite positive spectrum with adequate margin between the potential signatures for various faults. Thus the fault dictionary is being framed by tabulating the SD extracted for all three phases for the various test fault conditions. This fault dictionary is being used for fault diagnosis by the fuzzy classifier.

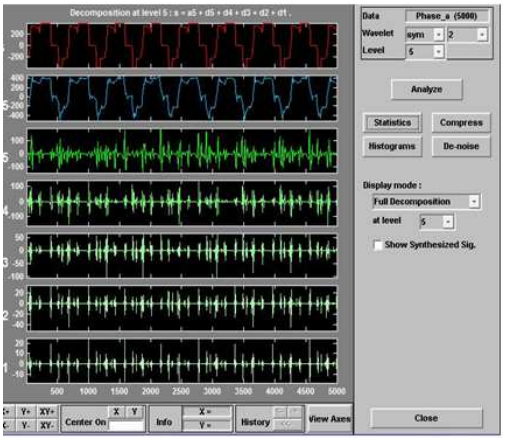

Fig. 7: Wavelet transform for phase A for fault OF4

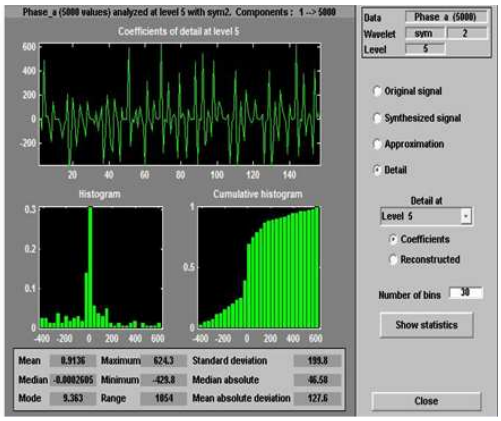

Fig.8: Statistical analysis of wavelet transform for phase A for fault OF4

The waveforms shown in Fig. 4 through Fig. 6 are subjected to statistical analyses. The wavelet transforms for phase A is shown in Fig. 7 and its statistical analysis tool outputs are displayed in Fig. 8. This wavelet transform and its statistical analyses for phase B and C can also be performed

Neural network classifier: Neural networks extraordinary tendency to learn from examples resembles the human thought process and intelligence (Manikandan and Devarajan, 2007; Prasannamoorthy *et al*., 2010; Duraisamy *et al*., 2007; Moussaoui *et al*., 2006). This enhanced the application of neural networks in fault diagnosis (Khomfoi and Tolbert, 2007; H.A. Abbassi, 2006; Benamrane *et al*., 2005; Fausett, 1994). It consists of training the net to respond in a specific manner to preset stimuli and gradually allow the network to learn to react to any fault condition. This eliminates the prerequisite of an extensive fault dictionary.

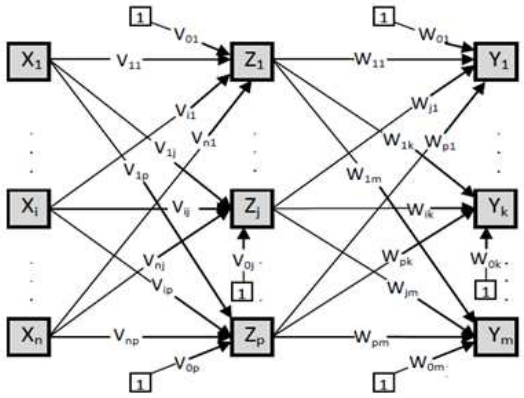

Fig. 9: Two layer BPN network topology

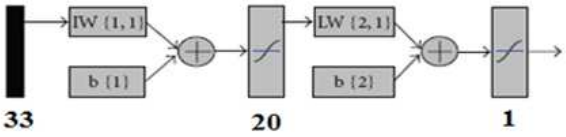

Fig. 10: Classifier for test circuit

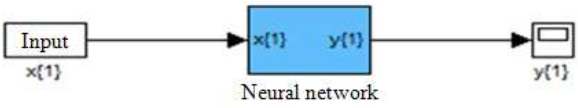

Fig. 11: Neural network classifier for single fault

Table 1: Fault dictionary for faults

Fault ID	Faulty Component	SD for phase A	SD for phase B	SD for phase C
FF	FF	186.70	186.60	186.40
SF1	T1	176.10	238.60	161.10
SF6	T6	174.20	186.30	255.00
OF1	T1	202.60	213.50	205.90
OF6	T6	180.50	199.30	210.00
OF12	T2, T5	209.00	207.70	166.90
OF15	T4, T6	203.50	211.50	175.30

FF- Fault Free; OF-Open Fault; SF-Short Fault

Further, the adaptive nature of neural networks ensures reliable performance even under adverse scenarios such as poorly designed models, noise and nonlinearities.

A neural network essentially consists of two or more layers. The layers are usually an input layer, an output layer and hidden layers in between. Each entity of a neural network is called a neuron. Each neuron in the network is necessarily connected to every other neuron. The relationship between two neurons is governed by weight. The weights are continually updated during the training of the net. The generalized delta rule was used during the training of the neural

network and also was employed for the fault diagnosis (HSU, 1992; Ma *et al*., 2007; Wahab and Mohamed, 2008; Alsabbah and Mughrabi, 2008). The Back-Propagation-Network (BPN) architecture was chosen. A typical BPN architecture is shown in Fig. 9.

The neural network used consists of 33 input layers and 1 output layer. The architecture was tried with one or more hidden layers which showed a marginal increase in the rate at which the learning curve of the net converged for an accuracy of as high as 10^6. However, it was noted that the curve was not smooth and hence a simple topology with just the input and output layers was implemented. Nevertheless, the capability of the network to identify faults was found to be without any compromise. The classifier for test circuit and neural network classifier for single fault are represented in Fig. 10 and 11 respectively.

Fault dictionary: The standard deviations extracted for all the three phases for the various test faults considered was then tabulated. The SD extracted for short circuit faults and open circuit faults are represented in Table 1. The Table may then be used as a fault dictionary in the classifier stage of the diagnosis.

MATERIALS AND METHODS

The model of the CUT was formulated using MATLAB 7.6. The output of which is subjected to wavelet analysis. The neural network classifier being built was utilized to effectively isolate and classify the faults.

RESULTS

The neural network was tested with six inputs, three of which were already made familiar to the net during the training stage (OF4, 12 and SF1) and the remaining three as test inputs (OF7, SF4 and 5), being completely unfamiliar to the network. The system was capable of analyzing the faults. The training performance plot for the classifier is shown in Fig. 12 and Table 2 represents the results obtained.

DISCUSSION

A novel method for fault diagnosis was in need to ensure the competent performance of the circuit under study. The suitability of wavelet analysis for the diagnosis of the fault using neural classifier has been illustrated well.

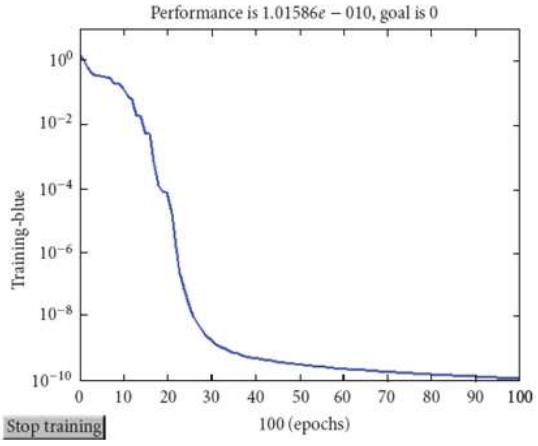

Fig. 12: Training performance plot for classifier

Table 2: Test results for fault diagnosis using neural networks

Switching states						Classifier Inputs			
T1	T2	T3	T4	T5	T6	SDa	SDb	SD_c	Fault ID
N	N	N	N	N	N	186.7	186.6	186.4	FF
N	N	N	O	N	N	199.8	213.4	199.6	OF4
N	O	N	N	O	N	209.9	207.7	166.9	OF12
N	N	N	O	O	N	176.1	238.6	161.1	SF1
N	N	S	N	N	N	200.1	205.0	173.4	OF7
N	N	N	S	N	N	172.8	230.1	151.8	SF4
N	N	N	S	N	N	253.6	180.0	178.3	SF5

N- Normal; O-Open S-Short

CONCLUSION

The proposed approach is found to be efficient in accurate identification and isolation of faults using fault dictionary. The approach is capable of identifying the fault without any ambiguity. But the time taken to complete the process is more. The disadvantages of prolonged processing duration in neural networks are effectively cancelled out in the presence of high performance processors.

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