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Low Transition-Generalized Linear Feedback Shift Register Based Test Pattern Generator Architecture for Built-in-Self-Test

[1]Sakthivel, P. and [2]A. Nirmal Kumar
[1]Department of Electrical and Electronics Engineering,
Velalar College of Engineering and Technology, Erode, Tamilnadu, India
[2]Department of Electrical and Electronics Engineering,
Information Institute of Engineering, Coimbatore, Tamilnadu, India

Abstract: Problem statement: In Built-In Self-Test (BIST), test patterns are generated and applied to the Circuit-Under-Test (CUT) by on-chip hardware; minimizing hardware overhead is a major concern of BIST implementation. In pseudorandom BIST architectures, the test patterns are generated in random nature by Linear Feedback Shift Registers. This normally requires more number of test patterns for testing the architectures which need long test time. **Approach:** This study presents a novel test pattern generation technique called Low-Transition Generalized Linear Feedback Shift Register (LT-GLFSR) and it was also called Bipartite GLFSR. Intermediate pattern (Bipartite technique) inserted in between consecutive test patterns generated by GLFSR was called LT-GLFSR technique which was enabled by a non overlapping clock scheme. Low-transition generalized linear feedback shift registers (LT-GLFSR), was used in a circuit under test to reduce the average and peak power during transitions. LT-GLFSR pattern generator would generate patterns with higher degree of randomness and high correlation between consecutive patterns would have efficient area implementation. LT-GLFSR did not depend on circuit under test and hence it could be used for both BIST and scan-based BIST architectures. **Results/Conclusion:** Simulation results show that this technique has reduction in power consumption and high fault coverage with minimum number of test patterns. The results also show that it reduces the peak and average power consumption during test for ISCAS'89 bench mark circuits.

Key words: Built-In Self-Test (BIST), Circuit-Under-Test (CUT), Low-Transition Generalized Linear Feedback Shift Register (LT-GLFSR), Design-For-Testability (DFT)

INTRODUCTION

Importance of testing in Integrated Circuit is to improve the quality in chip functionality that is applicable for both commercially and privately produced products. The impact of testing affects areas of manufacturing as well as those involved in design. Given this range of design involvement, how to go about best achieving a high level of confidence in IC operation is a major concern. This desire to attain a high quality level must be tempered with the cost and time involved in this process. These two design considerations are at constant odds. It is with both goals in mind (effectiveness and cost/time) that Built-In-Self Test (BIST) has become a major design consideration in Design-For-Testability (DFT) methods. BIST is beneficial in many ways. First, it can reduce dependency on external Automatic Test Equipment (ATE) because it is large, vendor specific logic, non-scalable and expensive equipment. This aspect impacts the cost/time constraint because the ATE will be utilized less by the current design. In addition, BIST can provide high speed, in system testing of the Circuit-Under-Test (CUT) (Pradhan *et al*., 2005; Pradhan and Gupta, 1991). This is crucial to the quality component of testing. (Chatterjee *et al*., 2003) discussed that stored pattern BIST, requires high hardware overhead due to memory devices required to store pre computed test patterns, pseudorandom BIST, where test patterns are generated by pseudorandom pattern generators such as Linear Feedback Shift Registers (LFSRs) and Cellular Automata (CA), required very little hardware overhead. However, achieving high fault coverage for CUTs that contain many Random Pattern Resistant Faults (RPRFs) only with (pseudo) random patterns generated by an LFSR or CA often requires unacceptably long test sequences thereby resulting in prohibitively long test time. In general, the dissipation of power of a system in test mode is higher than in normal mode operation. Power increases during testing

Corresponding Author: Sakthivel, P., Department of Electrical and Electronics Engineering,
Velalar College of Engineering and Technology, Erode, Tamilnadu, India

(Chatterjee, 1997) because of high switching activity, parallel testing of nodes, power due to additional load (DFT) and decrease of correlation (Chen and Hsiao, 2003) among patterns. This extra power consumption due to switching transitions (average or peak) can cause problems like instantaneous power surge that leads to damage of Circuits (CUT), formation of hot spots and difficulty in verification. Solutions that are commonly applied to relieve the extravagant power problem during test include reducing frequency and test scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time. The aim of BIST is to detect faulty components in a system by means of the test logic that is incorporated in the chip. It has many advantages such as at-speed testing and reduced need of expensive external Automatic Test Equipment (ATE). In BIST, a Linear Feedback Shift Register (LFSR) generates Pseudorandom test patterns for primary inputs (for a combinational circuit) or scan chain inputs (for a sequential circuit) (Girard *et al*., 2001) has given. On the observation side, a Multiple Input Signature Register (MISR) compact test set responses received from primary outputs or scan chain outputs (Zorian, 1993). But, BIST-based structures are very vulnerable to high-power consumption during test. The main reason is that the random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among adjacent bits within each pattern; hence the power dissipation is more in test mode.

Prior work: Pradhan and Chatterjee (1999) presented a GLFSR, a combination of LFSR and Cellular Arrays (CA), that can be defined over a higher order Galois field GF (2^{δ}), $\delta>1$. GLFSR's yield a new structure when the feedback polynomial is primitive and when ($\delta>1$) it is termed as MLFSR.

Corno *et al*. (2000) proposed a cellular automata algorithm for test pattern generation in combinational logic circuits. This maximizes the possible fault coverage and minimizes length of the test vector sequences. Also it requires minimum hardware.

A low power/energy BIST architecture based on modified clock scheme test pattern generator was discussed (Girard *et al*., 2001), it has been proposed that an n bit LFSR is divided into two n/2 bit length LFSRs. The fault coverage and test time are the same as those achieved in conventional BIST scheme.

Wang and Gupta (2002) presented a dual speed LFSR for BIST test pattern generation. The architecture comprises of a slow speed LFSR and a normal speed LFSR for test pattern generation. Slow speed LFSR is clocked by dual clocked flip-flop, this increases the area overhead than normal speed LFSR.

Pradhan and Liu (2005) have discussed an effective pattern generator should generate patterns with high degree of randomness and should have efficient area implementation. GLFSR provide a better random distribution of the patterns and potentially lesser dependencies at the output. EGLFSR is an enhanced GLFSR, using more XOR gate in a test pattern generator which achieves a better performance.

Nourani *et al*. (2008) deals with a low power test pattern generation for BIST applications. It exploits Low Transition LFSR which is a combination of conventional LFSR and insertion of intermediate patterns (bipartite and random Insertion Technique) between sequences of patterns generated by LFSR that can be implemented by modified clock scheme

Proposed work: This study presents a new test pattern generator for low- power BIST (LT-GLFSR), which can be employed for combinational and sequential (scan-based) architectures. The proposed design is composed of GLFSR and intermediate patterns insertion technique (Bipartite Technique) that can be implemented by modified clock scheme. The proposed technique increases the correlation in two dimensions: (1) the vertical dimension between consecutive test patterns (Hamming Distance) and (2) the horizontal dimension between adjacent bits of a pattern sent to a scan chain. Reducing the switching activity in turn results in reducing the average and peak power consumption, both peak and average (Pradhan *et al*., 2005). The GLFSR (Pradhan and Chatterjee, 1999) structure will be modified such that it automatically inserts intermediate patterns between its original pairs. The intermediate patterns are carefully chosen using bipartite techniques (Nourani *et al*., 2008) and impose minimal time to achieve desired fault coverage. Insertion of Intermediate pattern can be achieved based on non overlapping clock scheme (Girard *et al*., 2001). The Galois Field (GF) of GLFSR (3, 4) (Wen-Rong and Shu-Zong, 2009) is divided into two parts, it is enabled by non overlapping clock schemes. The randomness of the patterns generated by LT-GLFSR has been shown to be better than LFSR and GLFSR. The favorable features of LT-GLFSR in terms of performance, fault coverage and power consumption are verified using the ISCAS benchmarks circuits.

MATERIALS AND METHODS

GLFSR frame work: The structure of GLFSR is illustrated in Fig. 1. The Circuit Under Test (CUT) is assumed to have δ outputs which form the inputs to that GLFSR to be used as the signature analyzer (Pradhan and Chatterjee, 1999; Matsushima *et al*., 1997). The inputs and outputs are considered δ bit binary numbers, interpreted as elements over GF (2^{δ}).

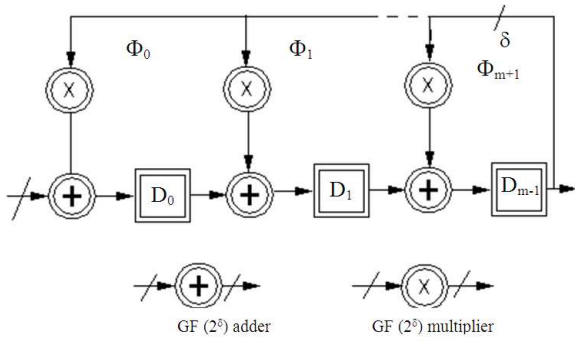

Fig. 1: The generalized GLFSR

The GLFSR, designed over GF (2^{δ}), has all its elements belonging to GF (2^{δ}). Multipliers, adders and storage elements are designed using conventional binary elements. The feedback polynomial is represented in Eq. 1 as:

$$\phi(x) = x^{m} + \phi_{m-1}x^{m-1} + ... + \phi_{1}x + \phi_{0} \quad (1)$$

The GLFSR has m stages, D_0, D_1...D_{m-1} each stage has δ storage cells. Each shifts δ bits from one stage to the next. The feedback from the D_{m-1}^{th} stage consists of δ bits and is sent to all the stages. The coefficients of the polynomial Φ_i are over GF (2^{δ}) and define the feedback connections.

The GLFSR when used to generate patterns for circuit under test of n inputs can have m stages, each element belonging to GF (2^{δ}) where (m×δ) is equal to n. A none zero seed is loaded into the GLFSR and is clocked automatically to generate the test patterns. In this study GLFSR with (δ>1) and (m >1) are used, where all possible $2^{m\delta}$ test patterns can be generated. The feedback polynomial will be a primitive polynomial of degree m over GF (2^{δ}). The polynomial from (Wen-Rong and Shu-Zong, 2009) can be described as in Eq. 2:

$$\phi(x) = (x + \beta^{2\delta 0})\left(x + \beta^{2\delta 1}\right)...\left(x + \beta 2^{\delta m-1}\right) \quad (2)$$

where, β is the primitive element of GF ($2^{m\times\delta}$). And construct Primitive polynomial of degree m over GF(2^{δ}) using (Eq. 2) is constructed with coefficients Φ_0, Φ_1.., Φ_{m-1} as powers of β, the primitive element of GF($2^{m\times\delta}$). Let δ =3,m = 4,(GF(3,4))The primitive polynomial GF(2^{12}) and GF(2^3) are denoted by β and α respectively in Eq. 3:

$$\phi(x) = (x + \beta)(x + \beta^{8})(x + \beta^{64})(x + \beta^{512}) \quad (3)$$

Expanding the polynomial as in Eq. 4:

$$\phi(x) = (x^{4} + \beta^{1755}x^{3} + \beta^{2340}x^{2} + \beta^{595}) \quad (4)$$

Solving the roots α of primitive polynomial p(x) Eq. 5:

$$p(x) = x^{3} + x + 1 \quad (5)$$

Is the primitive polynomial of GF (2^3), in GF (2^{12}), β^{1755} becomes an element which corresponds to a primitive element of GF(2^3) , α. Substituting the corresponding values, the feedback polynomial is as in Eq. 6:

$$\phi(x) = x^{4} + ax^{3} + a^{6}x^{2} + a^{5} \quad (6)$$

Storage element of the GLFSR are represented as:

$$D_1 = a_5X^2 + a_4x + a_3$$
$$D_2 = agx^2 + a_7x + a_6$$

And:

$$D_3 = a_{11}x^2 + a_{10}x + a_9$$

Respectively at each cycle, the values that are to be fed back into the storage elements are in polynomial:

$$(a_{11}x^2 + a_{10} + a_9)\phi_0$$
$$(a_{11}x^2 + a_{10}{}^x + a_9)\phi_1 + a_2x^2 + a_1x + a_0$$
$$(a_{11}x^2 + a_{10}{}^x + a_9)\phi_2 + a_5x^2 + a_4x +$$
$$a_3(a_{11}x^2 + a_{10}x + a_9)\phi_3 + a_9x^2 + a_7x + a_6$$

With the above explanations the generalize GLFSR in Fig. 1 is applied for GLFSR (3, 4) defined over GF(2^3) and its structure is given in Fig. 2.

Table 1 shows the first 15 states of the GLFSR (3, 4) with the initial seed "1111, 1111, 1111" and the GLFSR (1, 12), which is a 12 stages LFSR as a comparison.

Bipartite (Half-Fixed) technique (intermediate pattern insertion technique): The implementation of a GLFSR can be changed to improve some design features, such as power, during test. However, such a modification may change the order of patterns or insert new pattern (Nourani *et al*., 2008) that affect the overall randomness. For example, suppose that T^i and T^{i+1} are two consecutive patterns generated by an n-bit GLFSR.

The maximum number of transitions will be n when T^i and T^{i+1} are complements of each other.

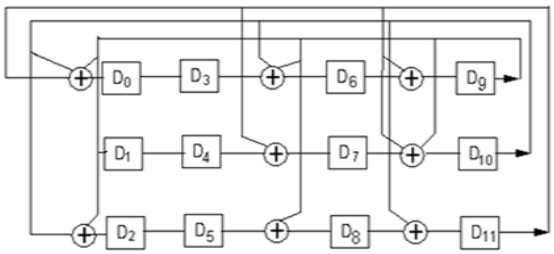

Fig. 2: Structure of GLFSR (3, 4)

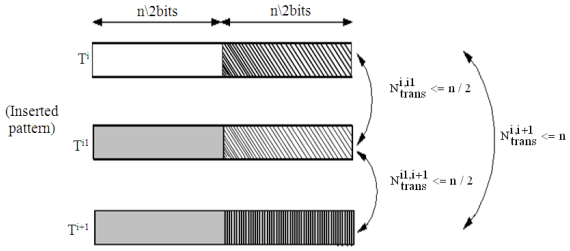

Fig. 3: Patterns insertion based on bipartite strategy

Table 1: First 15 states of the GLFSR

GLFSR (3, 4)	LFSR (n =12)
1111, 1111, 1111	1111, 1111, 1111
1101, 1110, 0010	0111, 1111, 1111
1011, 1001, 1101	0011, 1111, 1111
0111, 0100, 1111	0001, 1111, 1111
1100, 1111, 0100	1000, 1111, 1111
1111, 1011, 0100	0100, 0111, 1111
1111, 1101, 1100	0010, 0011, 1111
1111, 1101, 0001	1001, 0001, 1111
1001, 1110, 1100	0100, 1000, 1111
1111, 0001, 0111	1010, 0100, 0111
1101, 1111, 1111	0101, 0010, 0011
1101, 1010, 0010	1010, 1001, 0001
1011, 1001, 0101	0101, 0100, 1000
0111, 0100, 1110	1010, 1010, 0100
0100, 1110, 0010	0101,0101, 0010
1010,1011, 1101	1010,1010,1001

One strategy, used in (Zhang *et al*., 2001) to reduce number of transitions to maximum of n/2, is to insert a pattern T^{i1}, half of which is identical to T^i and T^{i+1}. This Bipartite (half-fixed) strategy is shown symbolically in Fig. 3.

Implementation of LT-GLFSR (Bipartite GLFSR) Technique: The proposed method for realizing a LT-GLFSR (Bipartite GLFSR) is discussed. Bipartite GLFSR is called as intermediate patterns inserted in between consecutive patterns generated by GLFSR which is enabled by non overlapping clock schemes. This technique inserts an intermediate test pattern T^{i1} between two consecutive random patterns (T^i and T^{i+1}) such that the transitions between T^i and T^{i1} and T^{i1} and T^{i+1} are reduced. In this technique, each half of T^{i1} is filled with half of T^i and T^{i+1} is shown in Eq. 7:

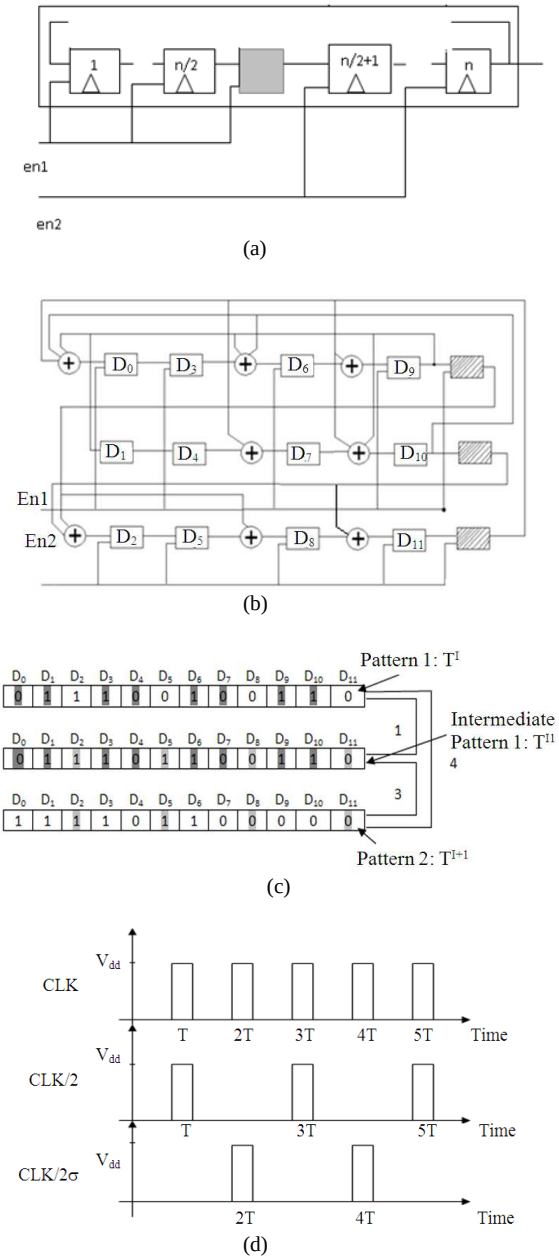

Fig. 4: (a) Bipartite LFSR (b) Architecture of Bipartite GLFSR (LT-GLFSR) (c) Bit Insertions in LT-GLFSR Bipartite Technique (d) Timing diagram of Enable signals

$$T^{i1} = \{t_1^i, ..., t_2^i, t_{\frac{n}{2+1}}^{i+1}, ..., t_n^{i+1}\} \quad (7)$$

In this method, a GLFSR is divided into two parts by applying two complementary (non-overlapping) enable signals (Wang and Gupta, 2002). In other words,

when one part is working, the other part is in idle mode. An LFSR including flip-flops with two different enable signals (Gizopoulos *et al*., 2000) is shown in Fig. 4a. The same concept used for GLFSR and Fig. 4b and c shows the architecture of the Bipartite GLFSR to generate intermediate pattern T^{i1}.

It has two non overlapping enable signals are En1 and En2. When En1En2 = 10, the first part of GLFSR is working, Idle mode part has to develop pattern as present state (stored value). Whereas, with En1En2= 01, the second part works. The additional Flip-Flops (shaded flip-flops) are added to the Bipartite GLFSR architecture to store the n, (n-1) and (n-2) th bits of GLFSR. First, to store the (n-1) and (n-2) th bits of GLFSR when En1En2 = 10 and send (n-2) th bit value into the XOR gate of D2 and D8 flip-flop and (n-1) th bit value into the XOR gate of D2 and D8 flip-flop when the second part becomes active En1En2 = 01.Second, to store the n^{th} bit of GLFSR when En1En2 = 01 and send its value into the XOR gate of D0,D4,D6 and D7 flip-flop when the second part becomes active En1En2 =10. Note carefully that the new (shaded) flip-flop does not change the characteristic function of GLFSR. The GLFSR's operation is effectively split into two parts; it is enabled by the two different enable signals as shown in Fig. 4d. This method is similar to the Modified clock scheme LFSR (Girard *et al*., 2001). They were used two n/2 length LFSRs with two different non-overlapping clock signals which increases the area overhead. Insertion of Intermediate pattern T^{i1} between two consecutive patterns generated by GLFSR (3, 4) T^i and T^{i+1}. Signals En1 and En2 select part of the GLFSR to generate random patterns as shown in Fig. 4c.This reduces the transitions from T^i and T^{i1} is equal to 1, from $T^{i1}$to T^{i+1} is equal to 3 and from T^i to T^{i+1} is equal to 4. The power consumption of LT-GLFSR itself is reduced due to using the Bipartite GLFSR technique. Only one part of the LT-GLFSR flip-flops are clocked in each cycle in conventional LFSR and GLFSR flip-flops are clocked at the same time in each clock cycle, thus its power consumption is much higher than LT-GLFSR. Table 2-6 show the power consumption of LFSR, GLFSR and LT-GLFSR for ISCAS bench marks circuits. Also it has better randomness of the patterns generated and increased correlation between consecutive patterns.

The following steps are involved to insert the intermediate patterns in between two consecutive patterns:

Step1: En1En2 = 01 the first part (D_0, D1, D3, D4, D6, D_7, D9 and D_{10}) of GLFSR is idle and the second part (D_2, D5, D8 and D_{11}) is in active mode. When there is no input bits change in first part the outputs will have its previous state (O0,O1,O3,O4,O6,O7,O9 and O10) as present state (stored value) and second part(D_2,D_5,D_8 and D_{11}) of GLFSR are sent to the outputs(O2,O5,O8 and O11) as next state. In this case, T^{i1} is generated.

Step2: En1En2 = 10 the first part (D_0, D_1, D_3, D_4, D_6, D_7, D_9 and D_{10}) of GLFSR is active and the second part (D_2, D5, D8 and D_{11}) is in idle mode. First part(D_0,D_1,D_3,D_4,D_6 , D_7,D_9 and D_{10}) of GLFSR are sent to the outputs (O_0,O_1,O_3,O_4,O_6,O_7,O_9 and O_{10}) as next state and No bit change in second part(D_2,D_5,D_8 and D_{11}) of GLFSR and sent to the outputs(O2,O5,O8 and O11) as present state(stored value). In this case, T^{i2} is generated.

Step 3: The process continues by going through Step 1 to generate T^{i+1}

Table 2: Test Patterns for first 20 states

Test pattern	LFSR	GLFSR	LT-GLFSR
1	111111111110	010001111010	111111111111
2	111111111000	111101101111	011100100110
3	111111100001	011111010000	101111011100
4	111110000111	100101010111	111101100000
5	111000011110	111100000101	101110011000
6	100001111001	100000010111	101001111000
7	000111100100	110011000010	000110111101
8	011110010000	000000101000	111011111010
9	111001000001	101000000000	000010111100
10	100100000110	101101111111	110011111000
11	010000011010	011101111000	010010111000
12	000001101001	101100010010	000101100000
13	000110100110	100101111111	001011000000
14	011010011000	010100000101	110110000101
15	101001100010	001101101000	001111000111
16	011000100101	101110111010	101000011011
17	100010010101	101100111010	000101111011
18	001001010111	001101111111	001011100011
19	100101011110	111001111010	110111000011
20	010101111000	010000010000	011011011011
21	010111100000	000010101000	010110100110

Table 3: Transition fault detected in S344

Pattern Generation	Number of test pattern	Pattern reduction (%)	Power (mW)
LFSR	167	--	83.0
GLFSR	36	21.75	65.2
LT-GLFSR	32	19.24	61.5

Table 4: Transition fault detected in S298

Pattern generation	Number of test pattern	Pattern reduction (%)	Power (mW)
LFSR	53	-	45.56
GLFSR	17	32.09	25.98
LT-GLFSR	12	22.67	21.23

Table 5: Transition fault detected in s386

Pattern generation	Number of test pattern	Pattern reduction (%)	Power (mW)
LFSR	796	-	35.8
GLFSR	83	10.4	28.9
LT-GLFSR	79	9.9	26.0

Table 6: Transition fault detected in s526

Pattern generation	Number of test pattern	Pattern reduction (%)	Power (mW)
LFSR	567	-	58.9
GLFSR	234	15.7	39.7
LT-GLFSR	197	12.4	31.6

RESULTS

The test patterns generated by LFSR, GLFSR and LT-GLFSR are used for verifying the ISCAS85 benchmark circuits S344, S298, S386 and S526. Simulation and synthesis are done in Xilinx 13 and power analysis is done using Power analyzer. The results in Table 3-6, are the test patterns for fault coverage and the reduction in the number of test patterns. Power analysis is carried out with the maximum, minimum and typical input test vectors for stuck-at faults and transition faults of sequential Circuits (CUT).

Modeling of the design is done in VHDL and simulation is carried out in Model Sim 6.5. Table 2 shows the first 20 states of the LT-GLFSR (3, 4) with the initial seed "1111, 1111, 1111" and which are 20 stages of LFSR and GLFSR for comparison.

DISCUSSION

Test patterns are generated by LFSR, GLFSR and LT-GLFSR and the analysis of randomness or closeness among the bit patterns are done. From the analysis the test patterns generated by LT-GLFSR has significantly greater degree of randomness, resulting in improved fault coverage when compared to standard LFSR and GLFSR. GLFSR is modified by means of clocking such that during a clock pulse one part is in idle mode and other part in active mode. This modification is known as LT-GLFSR which reduces transitions in test pattern generation and increases the correlation between and within the patterns by inserting intermediate patterns. From the discussed three methods the LT GLFSR has reduced test patterns with high degree of closeness and low power consumption for the CUT.

CONCLUSION

An effective low-power pseudorandom test pattern generator, LT- GLFSR is proposed in this study. Power consumption of LT-GLFSR is reduced due to the Bipartite GLFSR technique. Only half of the LT-GLFSR flip-flops are clocked in each cycle. LT-GLFSR's provide for greater randomness than standard LFSR and GLFSR, which have the potential to detect most stuck-at and transition faults for CUT with a fraction of patterns. This can be significance for the faults detection ISCAS circuits with a minimum number of input test patterns. The switching activity in the CUT and scan chains, their power consumption are reduced by increasing the correlation between patterns and also within each pattern. This is achieved with almost no increase in test length to hit the target fault coverage.

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