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DESIGN OF OPTIMAL CARRY SKIP ADDER AND CARRY SKIP BCD ADDER USING REVERSIBLE LOGIC GATES

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ABSTRACT

Reversible logic circuits have the ability to produce zero power dissipation which has found its importance in quantum computing, optical computing and low power digital circuits. The study presents improved and efficient reversible logic circuits for carry skip adder and carry skip BCD adder. The performance of the proposed architecture is better than the existing works in terms of gate count, garbage outputs and constant inputs. This design forms the basis for different quantum ALU and embedded processors.

Keywords: Low Power Circuits, Reversible Logic, Binary Coded Decimal Adder, Carry Skip Adder, Optical Computing

1. INTRODUCTION

Landauer (1961) proved that conventional combinational logic gates like AND OR disperse heat for every quantity of information that is destroyed while performing their operation regardless of the technology that is employed for accomplishing the circuit. According to his principle the energy dispersed for irreversible bit operation is given by KT ln2 (K-Boltzmann's constant and T-absolute temperature of the environment). Thus when the complexity of the circuit increases the energy dissipation becomes the major drawback factor.

The fundamental difference between irreversible circuits and reversible circuits is that the later doesn't lose any information. Bennett (1973) showed that only by applying the principle of reversibility to the circuits the zero power dissipation is possible. Thus reversibility concept will become an extremely important property in all future circuit design.

In computers, the most common numbering system is binary number system. However there is a need for Binary coded decimal number system in commercial, financial and internet based applications. This major importance arises from the fact that decimal numbers like 1.101 cannot be exactly represented with high accuracy in binary format and processing of these data is done using decimal arithmetic software (Cowlishaw, 2003). These factors specify the need for BCD in computers but it has its own drawback too. It is slower by 100 to 1000 times the binary arithmetic. This highlights the importance of both binary and BCD number system in their respective applications.

Adders are the basic building blocks in many computational units. There are different types of adders and the most commonly used adders are ripple carry adder, carry skip adder and carry look-ahead adder.

In the ripple carry adder the carry bit has to propagate through all the adder stages and this increases the delay of the circuit. By the introduction of carry look-ahead adders the carry bit is computed in parallel fashion, but they employ a large number of gates for computations. However, in this carry skip adder the propagation time is reduced by skipping over the group of adder stages (Islam *et al*., 2009) and presents hardware and performance compromise

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between carry look-ahead adder and ripple carry adder. So, faster adder circuits for binary and binary coded decimal have been investigated for several decades. The study continues the tradition by using reversible logic circuits for the design of carry skip adder and carry skip BCD adder. When compared in terms of gate count, garbage output and constant input, the proposed architecture performs better than the existing architectures.

1.1. Basic Denotations

1.1.1. Reversible Gate

A Reversible gate is an m-input, n-output (denoted by m×n) circuit that produces unique output pattern (Haghparast *et al*., 2008a) for each possible input pattern. A gate with i inputs and o outputs is said to be reversible if and only if i = o and there should be one to one correspondence between its inputs and outputs.

1.1.2. Garbage Output

The output of the reversible gate that is not used as a primary output or as input to other gates is called the garbage output. In short the unused output of a reversible gate (or circuit) is the garbage output (s). These garbage outputs are needed in the circuit to maintain the reversibility concept. It has a clear influence on the performance of the circuit and therefore should be minimized as much as possible. For example when the 4×4 HNG gate (Haghparast *et al*., 2008b) is used to perform the operation of full adder, the output vectors P = A and Q = B are the garbage output produced to preserve reversibility.

1.1.3. Quantum Cost

Quantum Cost of the circuit is calculated by knowing the number of basic reversible gates (gates of which cost is already known) needed to realize the circuit.

1.1.4. Constant Input

Input which is added to a n×n function for making it reversible is named as constant input. These input lines in the input side are either set to zero or one so as to bring the needed result. For example, consider the Feynman gate in which when any one input of the input line is set at constant 0, then the copy of an input bit is obtained and when any one input of the input line is at constant 1, then the inverted input bit is obtained.

1.1.5. Restrictions on Reversible logic synthesis

In designing reversible circuits Fan-out and Feedback or loops are strictly limited (Feynman, 1985). However these can be attained by the usage of additional gates like FG and BVF.

1.1.6. Reversible Peres Gate (PG)

The 3×3 (Peres, 1985) is described as follows: Input vector I_v = (A, B, C) and output vector O_v = (P = A, Q = A⊕B, R = AB⊕C). Block diagram of Peres is depicted in **Fig. 1**. Peres gate is the mixture of Feynman gate and Toffoli (1980) and this can implement operations like AND EX-OR. In this proposed design PG gate is used for performing AND operation.

1.1.7. Reversible Fredkin Gate (FRG)

Input and output vectors for 3×3 FRG (Fredkin and Toffoli, 1982) is defined as follows: I_v = (A, B, C) and O_v = (P = A, Q = B⊕AC, R = C⊕AB) FRG gate is depicted in **Fig. 2** and it is used in (Bruce *et al*., 2002) to construct ripple carry and carry skip adder circuits. This gate is used in the proposed designs for performing both AND and OR operation. This AND-OR output is obtained at output R.

1.1.8. Reversible MTSG Gate

Modified TSG (MTSG) gate is a 4×4 reversible gate (Biswas *et al*., 2008a) with following input and output vectors, I_v = (A, B, C, D) and O_v = (P = A, Q = A⊕B, R = A⊕B⊕C and S = (A⊕B). C⊕ (AB⊕D). This MTSG gate in **Fig. 3** can be used to realize a full adder by providing constant '0' at the input D.Quantum cost of reversible MTSG gate is 6 which is lower than 13 of TSG gate (Thapliyal *et al*., 2006).

This gate is used in the design so as to produce the sum, carry and the propagate output of the inputs.

1.1.9. MPS Gate

The reversible 5×5 MPS gate is further simplified and redrawn in **Fig. 4** and this works as a BCD detection and correction gate. This gate for performing the above operation does not use any constant input and produces zero garbage output. This gate detects the input that is greater than 1001 (9) and corrects it with correction factor of 0110 (6) to produce the final BCD output.

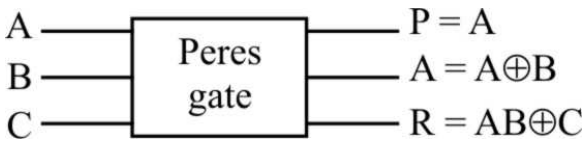

Fig. 1. Peres gate

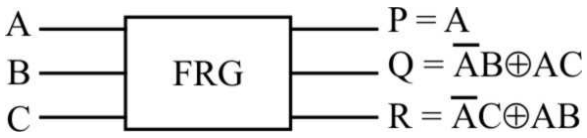

Fig. 2. Fredkin gate

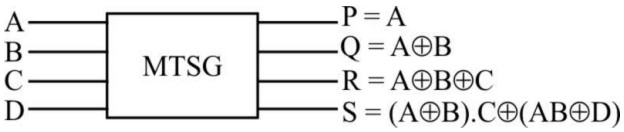

Fig. 3. MTSG gate

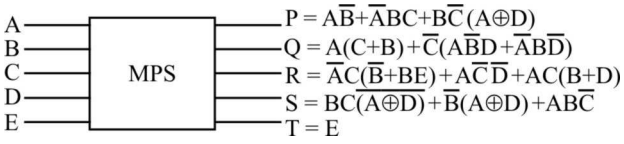

Fig. 4. MPS gate

2. MATERIALS AND METHODS

2.1. Proposed Reversible Carry Skip Adder

In the proposed carry skip adder in **Fig. 5**, 4 bit parallel addition is done by the modified TSG (MTSG) gate. The block propagate signal Z is generated using three Peres gate, where $Z = p_0.p_1.p_2.p_3$ and $p_0 = A_0 \oplus B_0$, $p_1 = A_1 \oplus B_1$, $p_2 = A_2 \oplus B_2$, $p_3 = A_3 \oplus B_3$.

Instead of Peres gate, even Toffoli gate can also be used for this purpose. But in this circuit Peres gate is preferred because of lower quantum cost when compared to Toffoli gate (Biswas *et al*., 2008a). The combined AND-OR function i.e., $C_{out} = ZC_{in} + C_4$ is done by the fredkin gate.

The algorithm of the proposed design is as follows:

Algorithm:

Reversible Carry-skip-adder (A,B,C_i)

Input:
Input Vectors: $A = (A_3,A_2,A_1,A_0)$ and $B=(B_3,B_2,B_1,B_0)$
Carry input : C_{in}

Output:
Output Vectors: $S = (C_{out},S_3,S_2,S_1,S_0)$

begin
Step1:
Compute propagate bit P_i for each adder block.
for (i = 0 to 3)
{
$P_i = A_i \oplus B_i$
}
$Z = P_o$ AND P_1 AND P_2 AND P_3
Step 2:
Compute $S_i = A_i \oplus B_i \oplus C_i$ for every adder block using the MTSG gate and $C_i = (A_i \oplus B_i)$. $C_{in} \oplus A_i B_i$ is generated for each adder block.
Step 3:
Evaluate the final carry output, $C_{out} = ZC_{in}+C_4$
end

2.2. Proposed Reversible Carry Skip BCD Adder

This proposed adder follows the same base architecture of proposed carry skip adder except that it includes a block for the BCD overflow detection and correction as depicted in **Fig. 6**. MTSG is used for the 4 bit parallel addition and produces the propagate bits (P_0, P_1, P_2, P_3) of its input in addition tosum and carry.

The carry skip logic block consists of three peres gate and one fredkin gate. The carry bit S_{out} is calculated based on the block propagate signal Z, carry in C_{in} and the most significant full adder carry bit C_4. i.e., $S_{out} = ZC_{in}+C_4$. The carry skip logic can improve carry propagation if the block propagate signal Z is equal to one. When Z = 1, the carry input C_{in} propagates to S_{out} regardless of the carry C_4. When Z = 0 then the carry C_4 propagates to C_{out} i.e., carry will be generated in ripple carry fashion.

This generation of C_4 will consume time and the AND-OR logic i.e., fredkin gate will wait for generating S_{out} until C_4 is resolved. Once after obtaining the carry S_{out} it passes through the MPS gate along with the intermediate sum i.e., (S_3, S_2, S_1, S_0). The single MPS gate acts as a BCD overflow detector and corrector gate. This produces the final BCD sum i.e., (C_{out}, F_3, F_2, F_1 and F_0).

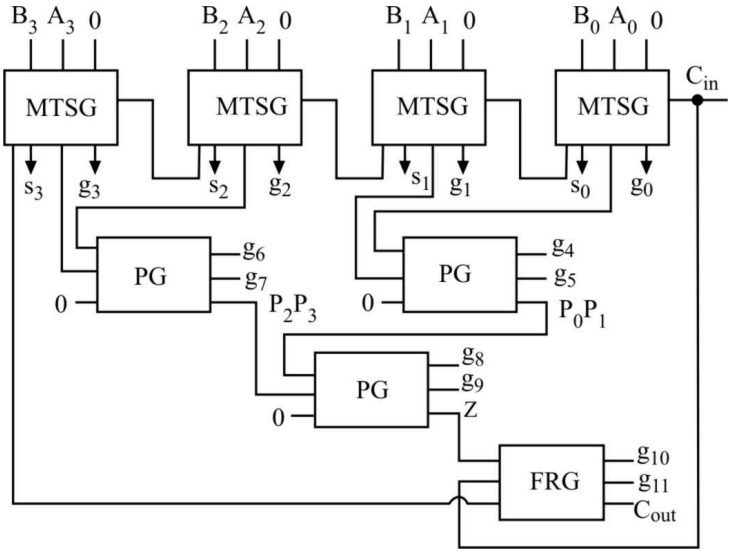

Fig. 5. Proposed carry skip adder

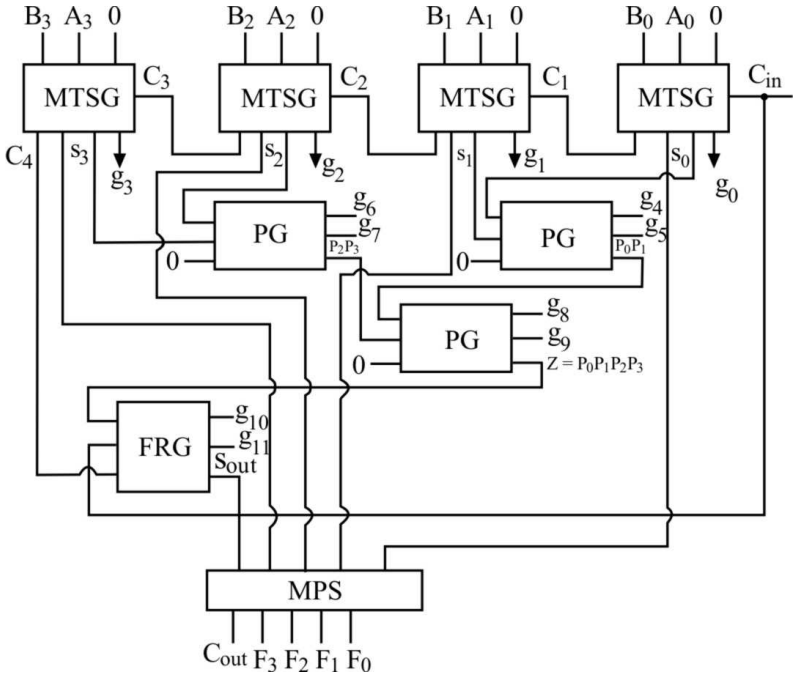

Fig. 6. Proposed carry skip BCD adder

3. RESULTS

The proposed reversible carry skip adder and reversible carry skip BCD adder circuits can be evaluated in terms of gate counts, constant inputs and garbage outputs produced. **Table 1** depicts the comparative analysis of different reversible carry skip adder circuits.

Evaluation of the proposed reversible carry skip BCD adder can be comprehended easily with the help of **Table 2**.

Table 1. Comparison of different carry skip adders

Designs in	Gate count	Garbage outputs	Constant inputs
(Islam *et al*., 2009)	14	19	15
(Bruce *et al*., 2002)	24	22	21
(Lala *et al*., 2010)	22	27	22
Proposed	8	12	7

Table 2. Comparisons of reversible carry skip BCD adders

Designs in	Gate count	Garbage outputs	Constant input
(Biswas *et al*., 2008b)	15	14	11
(Thapliyal *et al*., 2006)	15	27	13
(Islam *et al*., 2009; Biswas *et al*., 2008b)	15	14	11
(Islam and Begam, 2008)	15	36	24
(Bhagyalakshmi and Venkatesha, 2011)	13	14	10
Proposed	9	12	7

4. DISCUSSION

The **Table 1** clearly shows that in (Fredkin and Toffoli, 1982) full adder is constructed using 5 fredkin gates and it uses 4 constant inputs and produces 4 garbage outputs. Hence for 4 bit parallel addition it uses 20 fredkin gates, 16 constant inputs and produces 16 garbage outputs. This implementation in total requires 24 numbers of gates, uses 21 constant inputs and produces 22 garbage outputs.

Lala *et al*. (2010) New Full Adder (NFA) is constructed using 4R gates, uses 4 constant inputs and produces 4 garbage outputs. Therefore in total this circuit uses 22 numbers of gates, uses 22 constant inputs and produces 27 garbage outputs.

Islam *et al*. (2009) parity preserving gates are used for the construction of the circuit. This design is better when compared to the other designs in (Bruce *et al*., 2002; Lala *et al*., 2010) but the proposed design performs better than all the existing designs in every parameter.

It is evident from **Table 2** that the optimization parameters of designs in (Thapliyal *et al*., 2006; Islam and Begam, 2008) are computed with fan-out which in strict sense is restricted in reversible circuits and when reconstructed without fan-out it is sure that all the parameters will increase drastically when compared to the present results. Therefore from **Table 2** it is obvious that the proposed design performs better the existing designs in all parameters.

5. CONCLUSION

In the study an optimized carry skip adder and carry skip BCD adder are presented. It is clearly found that both circuits are highly optimized in terms of gate count, constant input and garbage output when compared with the existing designs. These optimized parameters will have a direct effect on the total cost of the circuit. These types of adders will be definitely useful in constructing larger computational structures and in future computers.

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